AN ELECTRICAL POWER SYSTEM IMPLEMENTING FIXED POWER POINT TRACKING WITH TEMPERATURE COMPENSATION

by

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ABSTRACT

For the past decade Montana State University (MSU) researchers have been developing a Radiation Tolerant Computing System (RTCS) to support the National Aeronautics and Space Administrations (NASA) technology road map for space technology. The next iteration of this effort is a free flying CubeSat being developed in the Electrical and Computer Engineering Department named RadSat-g. This thesis addresses the Electrical Power System (EPS) of the satellite avionics in support of RTCS for RadSat-g. One of the main problems that CubeSat developers face is the small amount of solar power generated due to available space for solar cell placement on the small frame of a CubeSat. Charging the battery from the solar panels generally employ one of two types of energy transfer methods, direct energy transfer and power point tracking. Direct energy transfer's disadvantage is the strings of solar cells need to be tuned to the battery and as such has the potential to leave valuable space on the solar panel unused. Power point tracking has the advantage of the ability to utilize variable string lengths, this allows each solar panel to have the maximum number of cells and therefore exploit the maximum available power. In terms of CubeSat power availability, the RTCS has a substantial power requirement, so power point tracking is required for the satellite to be power positive. To accommodate this requirement, a new EPS needed to be researched, designed and built. This new EPS, named Phoenix v2.3 EPS, meets the needs of the RadSat-g mission while leveraging components with flight heritage from past MSU Space Science Engineering and Laboratory missions.

INTRODUCTION

As technology advances, more space based assets are launched into orbit to provide everyday services. These systems must be reliable and long lasting. A problem arises in this environment because any object in space is subject to harsh radiation. The spectra of radiation ranges from low energy particles to high energy gamma rays. Radiation causes faults in sensitive electronic circuitry, which can lead to expensive failures. Radiation effects on electronic hardware are categorized as Total Ionizing Dose (TID) and Single Event Effects (SEE) [1]. TID failures are from a long exposure of low energy radiation. SEE radiation failures are from high energy particles. As the SEE particles pass through the semiconductor substrate, electron-hole pairs are created. These electron hole pairs can induce a transient voltage spike, which can cause either hard or soft errors. A soft error is characterized by if the SEE changes the state of bits in memory or causes the processor to execute erroneous operations. This is called a Single Event Upset (SEU). SEU's can be fixed with error checking or processor resets. A hard error is destructive and causes permanent damage. An example of a hard error is a latch-up. A latch-up creates a low impedance path across a Metal-Oxide Semiconductor Field -Effect Transistor (MOSFET) circuit triggering an over-current situation. If not caught, the transistors breakdown permanently. A few types of radiation mitigation have been devised such as shielding and radiation hardened parts, but these can be prohibitively expensive.

An SEE mitigation technique has been explored at Montana State University to reduce cost and increase reliability of radiation tolerant systems [2]. This mitigation technique is implemented on the Radiation Tolerant Computer Stack

(RTCS) technology demonstration. The RTCS corrects SEE upsets automatically in real time so that computational time is not lost. The radiation tolerance comes in the form of software and redundancy, not in physical hardware. This substantially reduces cost because consumer off the shelf (COTS) Field Programmable Gate Arrays (FPGA) can be used.

The radiation tolerant computer stack uses an FPGA broken into nine redundant processing tiles. Each of the identical nine tiles house a soft processor. The soft processor is a 32-bit RISC MicroBlaze from Xilinx. The soft processors each run the desired program in parallel. Each tile can be partially reconfigured if an upset occurs. To find upsets the computer stack uses a time tested process, Triple Modular Redundancy (TMR), which was first used in 1950 on the computer SAPO [3]. TMR voting detects faults in one of three active tiles by looking at the three simultaneous outputs and voting for the two outputs that are the same and rejecting the one that is different. When a tile is found to be corrupted, one of the other six tiles (reserved as spares) is brought online. The corrupted tile is then partially reconfigured and becomes an inactive tile ready to be brought online in the future. The inactive tiles are also compared against a known state to detect faults that might have occured from an SEE in the unused fabric of the FPGA. This is done to have a correctly functioning processor when activating a needed replacement tile. The main FPGA running the redundant tiles is an Artix-7 from Xilinx with a Spartan-6 FPGA acting as the controller.

The Radiation Tolerant Computer Stack, shown in Figure 1.1, has been under development at MSU starting in 2007. The development has undergone cyclotron tests, high altitude balloon flights, sounding rocket missions, and a current long term in situ radiation exposure test on the International Space Station (ISS). The current iteration was delivered on December 9, 2016 to the ISS via the HTV-5 resupply mission lauched out of the Tanegashima Space Center in Japan. The current RTCS is being tested in the NanoRacks internal eperiment locker [2]. Weekly data downlinks from the ISS show the RTCS is still functioning correctly and collecting data.

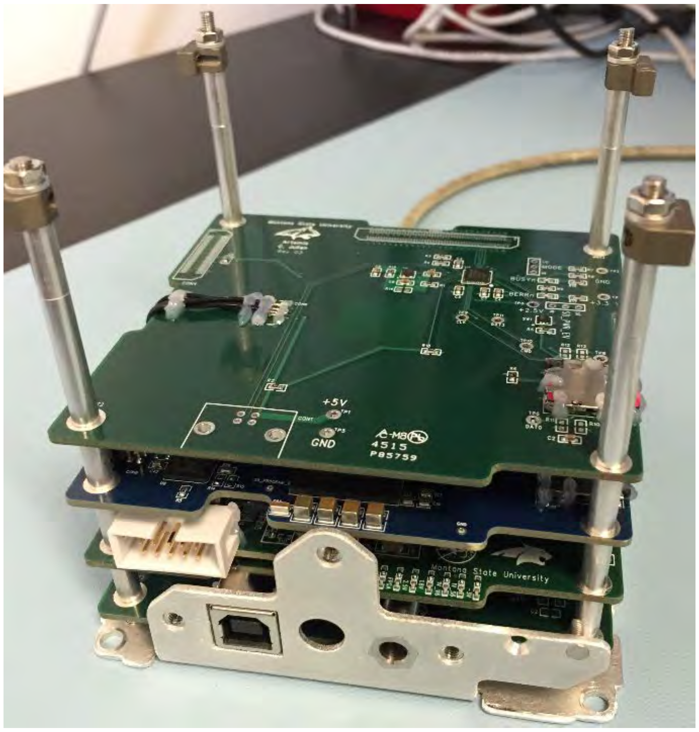


Figure 1.1: The RTCS configured for Artemis

The next iteration of this technology demonstration will be a free flying CubeSat mission. A free flying satellite allows for the RTCS to be immersed in a more severe radiation environment than what the ISS can provide. This free flying satellite is called RadSat-g. RadSat-g is a CubeSat which has been selected by the CubeSat Launch Initiative for launch in early 2018 to be deployed from the ISS. The technological challenge of RadSat-g over the current ISS experiment is that on the ISS the system has access to power and communications, while RadSat-g must be completely self reliant. This means that an avionics stack is required to control power, command and data handling, and communications. The avionics stack must be integrated with the RTCS to form a functional satellite. To build RadSat-g, existing technology was leveraged from Montana State's Space Science and Engineering Laboratory (SSEL). The SSEL's FIRBIRD avionics stack was modified to fit the unique requirements of the RTCS and the mission objectives. The FIREBIRD mission (Focused Investigations of Relativistic Electron Burst Intensity, Range, and Dynamics) is designed to collect information on the spatial size and energy dependence of electron microbursts in the Van Allen radiation belts.

The main modification from the FIREBIRD Avionics stack was the Phoenix v2.1 Electrical Power System. While the regulators and processor stayed the same for RadSat-g's Phoenix v2.3, the solar panel energy transfer to the battery had to be modified to meet the requirements. The Phoenix v2.1 used direct energy transfer to charge the battery from the solar panels, however, due to the increased power requirement from the RTCS, the Phoenix v2.3 EPS now uses Fixed Power Point Tracking allowing for an additional $\sim$1 W orbit average power over the direct energy transfer counterpart.

MOTIVATION

We have come a long way since 1957 when Sputnik launched from Gararin's Start [4]. The rapid advancement of technology from the dawn of the space age until now has been an arduous process. In 1999 when Professor Bob Twiggs and Jordi Puig-Suari proposed the CubeSat [5], the main driving entities advancing space technology were agencies such as National Aeronautics and Space Administration (NASA) and European Space Agency (ESA). Due to the expensive nature of space missions, the technology used needed to be sound before launch. This meant many years of development and testing before a technology was allowed to be on a spacecraft, which in turn meant high cost. The CubeSat changed that. Now universities have a relatively inexpensive path to space access so high-risk, high-reward missions can be justifiably flown. The concept of the CubeSat started as a way to teach the next generation of engineers the process that they might encounter working the aerospace sector. However, this quickly evolved into something much more than just education. CubeSats began to be used for meaningful science missions and technology demonstrations. The technology demonstrations are used to increase their Technology Readiness Levels (TRL) as a proving ground for use on future more expensive missions. This new avenue of development allowed for a another golden age of space technology.

What is a CubeSat

A CubeSat is a class of small satellite that usually gets launched as a secondary payload on a satellite deployment mission or from the International Space Station. If depoyed as a secondary payload, they are launched with a primary satellite, therefore they are usually subject to the requirements and trajectory of the main mission. The

CubeSat class is defined in terms of "U's" with a 1U being 10 cm x 10 cm x 10 cm in volume with mass not to exceed 1.33 kg per U. Multiple U's can be stacked together giving larger satellites such as a 3U (10 cm x 10 cm x 30 cm) or a 12U (20 cm x 20 cm x 30 cm) [6]. As of July 2017 the total number of CubeSats that have been launched reached 764 [7]. CubeSats are no longer simply a learning or research tool for universities, but are being used by industry for commercial applications. CubeSats allow for missions that would otherwise be prohibitively expensive. The ability to launch a cluster or swarm of CubeSats for multi-point measurements can even give CubeSats an advantage over traditional science missions.

Anatomy of a CubeSat

Every CubeSat, regardless of whether it is a 1U or a 12U [6], needs a structure, electrical power system, a way to make decisions, and a purpose. Figure 2.1 shows IT-SPINS, a typical 3U satellite, built at Montana State University for space weather investigations. All of these subsystems need to work in unison to achieve mission success. CubeSats are inherently single point of failure devices, meaning if one of the subsystems fails, the entire satellite fails. Due to their small size, there is not enough volume, weight, or budget available to have redundant systems on most CubeSats. Therefore, these systems fall into a class of high-risk, high-return satellites. As such, CubeSats are a perfect platform for technology demonstrations. MSU has been developing CubeSats to support its research with missions such as IT-SPINS, FIREBIRD, and most recently RadSat-g.

Structure Every satellite needs some sort of structure to provide mechanical support. There are many consumer off-the-shelf solutions (COTS) such as the Pumpkin Chassis [8] or the Canisterized Satellite Dispenser (CSD) Chassis [9]. Each of these come with a different deployment mechanism that will influence what type of

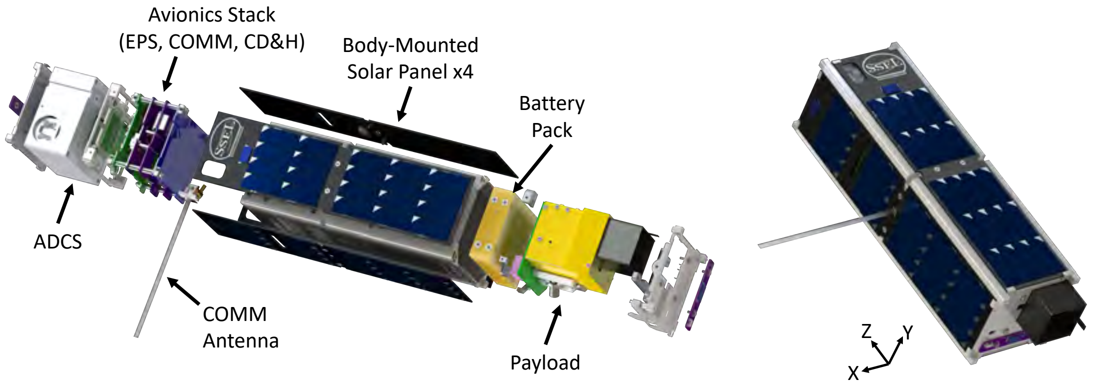


Figure 2.1: IT-SPINS Exploded View

orbits the satellite can go in as well as having their own set of mechanical requirements. Every chassis will, however, need to be modified to fit the needs of the mission, whether that is mounting holes or sensor cutouts. This lends to the theme in CubeSat design that it is nearly impossible to just buy COTS parts without some sort of modification to fit the mission requirements.

Other elements of the structure besides the chassis is the antenna system. Every satellite needs to be able to communicate with the ground to download its information. For most satellites operating in the amateur bands this means a 70 cm dipole or monopole antenna, which has to be deployed. The antenna deployment is another single string failure mode. If the antenna does not deploy the mission is a failure. For the recent satellites that Montana State University has deployed into orbit, they all use a burn wire configuration that melts a mono-filament using a nichrome coil of wire. Even though this is a structural element, it is influenced by the communications requirement of a quasi-symmetric ground plane for an acceptable far-field radiation pattern of the antenna. It is easy to see that the structure is influenced by all other subsystems and as such needs careful consideration.

Power Systems The Electrical Power System is comprised of the power generation units, such as solar cells, an energy storage system, and the power distribution system. The approximate 90 minute orbit of RadSat-g will expose the solar panels to the sun for 60 minutes and will be in eclipse for 30 minutes. During the 60 minute time in the sun the satellite must re-charge what was depleted during the eclipse as well as power the system. The EPS must be able to take solar power and convert it to the appropriate levels to store or use it. This involves power conditioning, whether it is direct energy transfer or some form of power point tracking (PPT). Direct energy transfer is when the cells are connected to the battery via a single diode. If this method is used, all the the strings of solar cells must be balanced and care must be taken to match the cell voltage to the nominal battery voltage. If power point tracking is used, then any number of cells can be used in a string because the PPT electronically takes care of the balancing. The EPS must then convert the voltage of the battery to the necessary voltages for the other subsystems in the spacecraft. The EPS also handles turning on and off subsystems if necessary as well as gathering telemetry such as current usage, charge status of the battery, or temperatures of the regulator or batteries. For MSU satellites, the telemetry gathering is from an on board computer system.

Command and Data Handling The Command and Data Hanedling (CD&H) controls the overall operations of the satellite. The main software for the satellite runs on the CD&H processor, which in the case of MSU satellites is a real-time operating system. Once it boots, the program runs the command sequences, which are stored on a NOR flash module. Command sequences are the way the satellite is automated and can be changed in orbit by uploading new ones. There are timers that run the other routines in the satellite such as the beacon, the radio, or gathering telemetry.

For many CubeSats, they are only in contact with the ground for 10 minutes a couple of times a day, so the satellite needs to be autonomous most of the time. This means gathering science/engineering data and storing it for future down-link. The CD&H can also handle the NAND memory module if it is not broken out on another board. The NAND handles the large data-storage with the data surviving over power resets. The CD&H processor also utilizes telemetry monitors. Telemetry monitors check the data in the Space Craft Data Base (SCDB) once a second. If a value reaches a preset threshold, a command sequence is triggered. This process can be used for safe-modes and other time sensitive tasks. For the Safe-Mode, if the battery voltage reaches the low threshold, the cadence of the beacons are reduced and the payload is turned off until the battery returns to a safe voltage level.

Communication CubeSats do not get retrieved, instead, they burn up in the atmosphere. This means any data that is required from the satellite needs to be transmitted to the ground. CubeSats operate in different frequency bands, the most popular of which is the UHF amateur radio band for university based CubeSats [10]. As CubeSats get more complicated, different bands that allow more data throughput are required. The communication system must be able to both receive and transmit the data during the approximate 10 minute passes. MSU satellites down-link at 19k2 baud, but with an effective baud rate of about 6k baud due to timing of packets and buffering in the radio. This needs to be taken into account when creating a data budget, which guides what kind of data is absolutely required to get to the ground to meet the science/technology goals of the mission.

There are other rules that the communication system must abide by such as a maximum of -152 dBW/m2/4kHz Isotropic Signal Level at the groundsation to limit RF noise poution [11]. This limits the transmit power of the radio based of its altitude

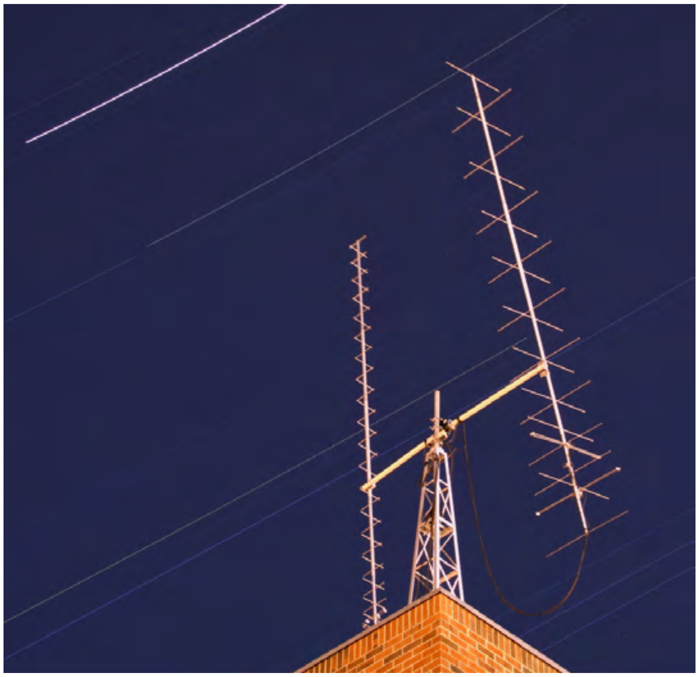


Figure 2.2: The MSU Ground Station

and antenna type. These rules are imposed on the CubeSat by agencies such as the Ferderal Communications Commission or the International Amateur Radio Union (IARU). The IARU grants access to allocated amateur bands that are subject to change, for example FIREBIRD I up-linked on the 2m band, but on July 1 2014 they no longer accepted frequency coordination requests on this band for experimental satellites [12]. Each satellite must go through frequency coordination with the IARU and once that is complete then get FCC Licensing and comply with their rules.

GroundStation The complementary pair to the communication system is the ground station. It is the earth based portion of the communications link. Besides controlling the rotor to move the antennas to track the satellite, the ground station must have the ability to decode the packets from the satellite, usually using a software defined radio (SDR). MSU's ground station antennas can be seen in Figure 2.2. The left antenna is the UHF circularly polarized receive antenna and the right antenna is the circularly polarized VHF transmit antenna. To keep the received power constant while the satellite is tumbling, the spacecraft antenna is linearly polarized while the ground antennas are circularly polarized.

The ground-station automatically decodes the beacon packets that the satellite sends out at some cadence depending on what was determined during the Concept of Operations (ConOps) design. Once the beacon has been decoded, decisions need to be made such as whether there is enough energy in the batteries to have a data download or if the CubeSat should be placed in a safe mode. If it is determined to be safe to get a data transmission from the satellite, then the ground station will up-link a command to the satellite to retrieve data out of memory and down-link it during the remaining of the pass. If other communications methods are used, such as the Globalstar network, then a ground station is not needed because the data channel is through the service provider.

The remaining chapters in this thesis will focus on the EPS, which was my contribution to the RadSat-g mission.

SYSTEMS ENGINEERING OF RADSAT-G

RadSat-g

RadSat-g is a 3U technology demonstration satellite built in the Electrical and Computer Engineering Department at MSU. Its purpose is to demonstrate a novel radiation tolerant computer system that has been in development at MSU for the past decade. RadSat-g leverages technology created by the Space Science and Engineering Lab in the Physics Department at MSU. The avionics section of RadSat-g is based on SSEL's FIREBIRD mission, a pair of satellites currently operating in orbit, with some modifications. The main payload of RadSat-g is a Radiation Tolerant Computer Stack, which currently is being tested on the International Space Station [2]. An exploded view of RadSat-g is shown in Figures 3.1 and 3.2. RadSat-g is the latest demonstration to advance the Technology Readiness Level (TRL) of this computer technology and a successful launch of RadSat-g will increase the TRL level of the RTCS to TRL 8 or 9. RadSat-g will be carried to the ISS on a commercial resupply mission and then put into orbit using the NanoRacks CubeSat Deployer in 2018.

Payload

The RTCS is comprised of three boards; the RTCS Power Board, Data Logging Board, and the FPGA board. The main computer for the payload is housed on the FPGA Board and contains a Xilinx Artix 7 and a Spartan 6 FPGA. The purpose of the RTCS is to provide a COTS hardware with custom software solution for radiation mitigation. The fabric of the FPGA is broken up into nine tiles which all are configured to have identical MicroBlaze soft processors from Xilinx. Three of the tiles are simultaneously active and running the desired code. When a Single Event Upset (SEU) occurs in the FPGA the software architecture finds the fault using a Triple

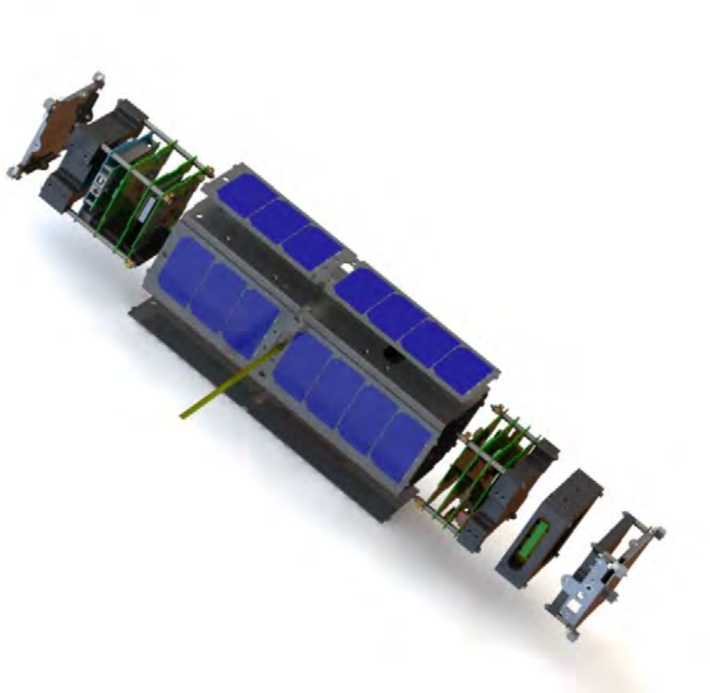


Figure 3.1: Exploded view of RadSatg

Modular Redundancy (TMR) architecture and activates one of the spare tiles. The tile that was affected by the SEU will be partially reconfigured in the background to repair the fault and becomes one of the spare six tiles ready to take over a primary tile. Currently the test mode is to manually inject faults in the fabric to confirm the FPGA switches tiles correctly. Each time a fault is injected, a fault counter in incremented. When a real fault occurs, the fault counter is incremented and the expected value of the faults will be different, indicating a radiation fault that was recovered by the RTCS [2]. The RTCS uses its own power board, so the EPS is only required to provide un-interrupted unregulated power. The RTCS must run continuously without power interruption to meet the requirement from the mission objectives. The data is passed over an RS422 connection between RTCS and the Multi-Function Interface Board (MFIB), which stores the packet in memory for future downlink.

Exploiting Flight Heritage of Previous MSU CubeSats

”Heritage” refers to a CubeSat subsystem that has already been used in a space mission. Heritage allows for rapid technology development and reliability. Space based hardware is impossible to fix once in orbit; therefore, the design must be sound. Also, due to the nature of the tight schedule for a launch of a CubeSat mission, the designs require rapid prototype development that can only be achieved if leveraging the work done by predecessors. There are two types of heritage, full subsystem and component level heritage. Full subsystem heritage has no modifications and are flown as is, while component level heritage is utilized when modifying an electrical design or creating a new one.

RadSat-g leverages heavily on subsystem heritage. Other than removal of the USB interface board, the RTCS is the same payload operating on the International Space Station as part of its current mission [2]. The CD&H from pumpkin is a re-flight system from the FIREBIRD missions with some code modifications to remove unneeded functionality and add the requirements of the RTCS. Component level heritage was used in the design of the MFIB and EPS subsystems which needed substantial changes over the FIREBIRD missions. This was caused by the necessity to fulfill flow down requirements of the RTCS. The communication system is the only non-heritage subsystem due to a frequency allocation rule change governed by the International Amateur Radio Union. The batteries are also heritage, although the configuration changed from a 2S1P (two cells in series) for the FIREBIRD mission to a 2S2P (two pairs of cells in parallel and each pair connected in series), configuration for RadSat-g to increase the capacity needed by the RTCS. The heritage radio changed from the Astrodev Helium to the Astrodev Lithium, however the same manufacturer was chosen to minimize the necessary code changes.

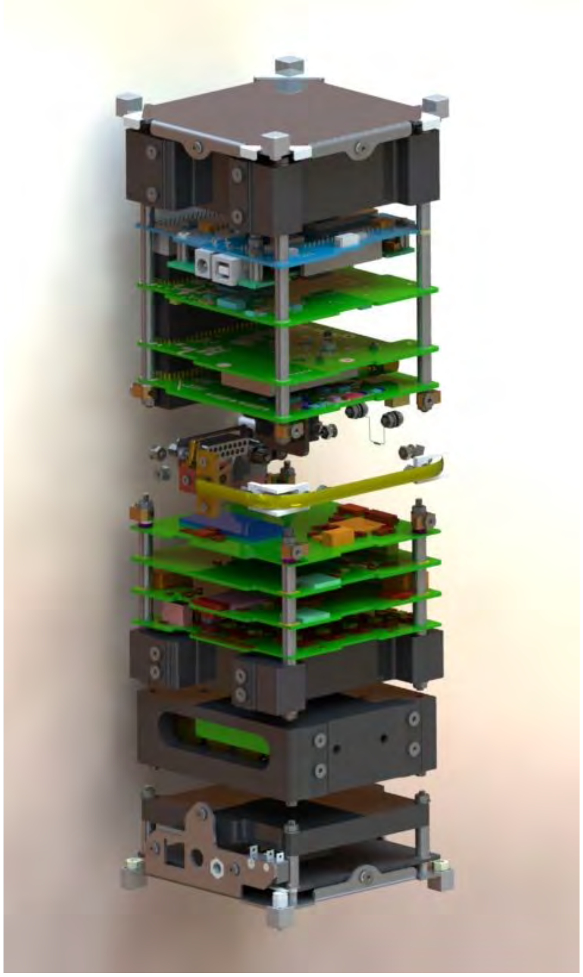


Figure 3.2: Inside view of RadSatg

Requirements

The requirements for the mission come from the Requirements Verification Matrix (RVM). The requirement flow down is also used to determine if the mission meets the criteria for success after launch. The RVM is carefully designed in order to ensure mission success and each requirement flow down is in support of the main mission objectives.

Shown in Figure 3.3, the requirement flow-down starts with the M0-1 (Mission Objective) and flows down to M-1 through M-4 (Mission Requirements), as shown

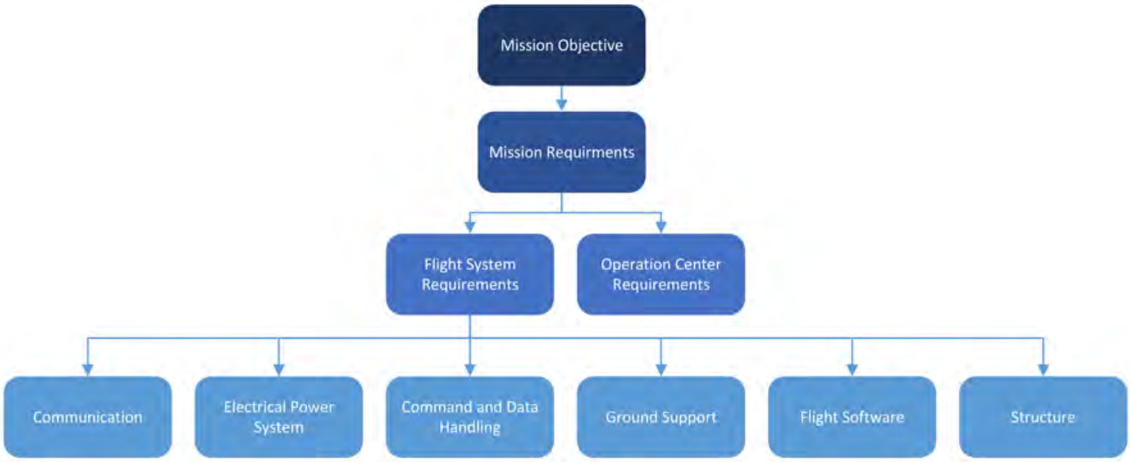
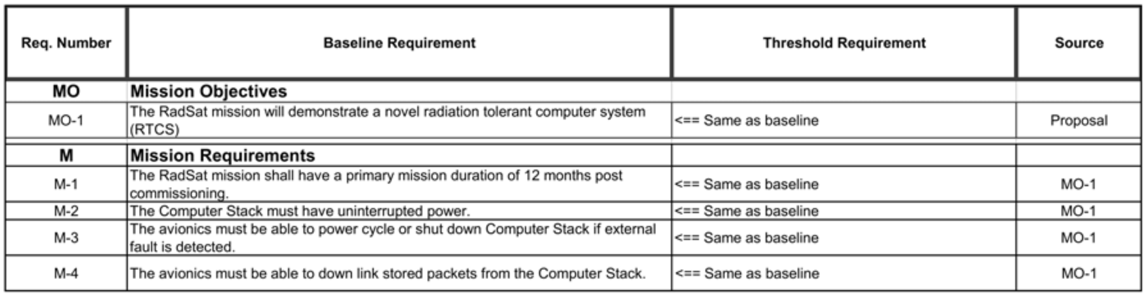

Mission Objective
Mission Requirments
Flight System Requirements
Operation Center Requirements
Communication
Electrical Power System
Command and Data Handling
Ground Support
Flight Software
Structure

Figure 3.3: RadSat-g Avionics Section Flowdown

in Figure 3.4. Once the Mission Requirements have been constructed the Flight System Requirements, Figure B.1, are constructed to accommodate the Mission Requirements. Requirement flow down guides the decisions in the design and are carefully written to insure nothing is missed before the satellite's design review. A feature required for mission success can be overlooked if not properly documented.



Req. Number	Baseline Requirement	Threshold Requirement	Source
MO	**Mission Objectives**		
MO-1	The RadSat mission will demonstrate a novel radiation tolerant computer system (RTCS)	<== Same as baseline	Proposal
M	**Mission Requirements**		
M-1	The RadSat mission shall have a primary mission duration of 12 months post commissioning.	<== Same as baseline	MO-1
M-2	The Computer Stack must have uninterrupted power.	<== Same as baseline	MO-1
M-3	The avionics must be able to power cycle or shut down Computer Stack if external fault is detected.	<== Same as baseline	MO-1
M-4	The avionics must be able to down link stored packets from the Computer Stack.	<== Same as baseline	MO-1

Figure 3.4: Mission Objective and Requirements Flow-down

The MO-1 requirement states that the RadSat-g satellite is a technology demonstration and therefore the mission requirements are constructed to reflect the technology demonstration nature of the mission. M-1 though M-4 are in support of the RTCS mission objective. M-1 is the lifetime requirement to satisfy the necessary time to show the RTCS can mitigate radiation effects on the computer stack. A deviation from heritage comes from M-2 “The Computer Stack must have uninterrupted power.” Previously every subsystem would have a watchdog timer (WDT) power reset every approximately twelve hours that would power cycle the entire CubeSat for approximately 10 seconds. The WDT is used to mitigate upsets, which the RTCS is designed to do, so if the power on the RTCS was not continuous it would invalidate the RTCS test. M-3 requires the ability to command an interrupt in the power to the RTCS. This is a backdoor to power-cycle the RTCS because if it gets in an un-anticipated state there must be a way to reset the RTCS to a known state. M-4 is a communication and memory requirement that the data must be able to be transmitted to the ground to verify the desired functionality of the RTCS. These requirements flow into the Flight Requirements, which in turn flow into each subsystem such as the Electrical Power or Communication Systems. The Mission Requirements also flow into the operation centers requirements. Once the high-level requirements are derived, the four design budgets are constructed to help guide the rest of the requirement flow-down.

Design Budgets

Each of the four budgets influence one another and balance in all budgets are necessary to meet the requirements of the mission. An example would be if the mission requires a large amount of telemetry, then the radio would be required to have a higher baud rate to downlink the collected data. This in turn makes the link budget demand more power from the radio. With the radio operating more, the power budget will have to compensate for the higher orbit average required power. This would require more battery capacity to survive eclipse. The increased battery capacity would require more batteries which in turn increases the mass of the CubeSat.

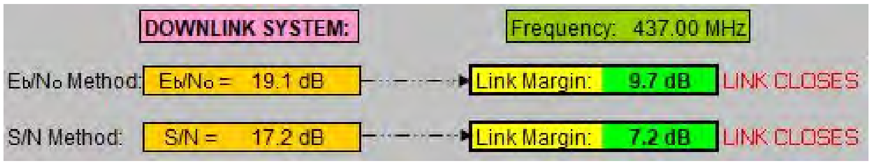
Each mission can have a driving budget based off of a mission requirement, which cannot be compromised, and the other budgets must compromise. In the case of RadSat-g it does not require a large amount of telemetry, but the payload needs to be continuously operating and the RTCS requires a substantial fraction of the available power generated for a 3U CubeSat. The continuous operation of the RTCS is a Mission Requirement (M-2) in support of the Mission Objective, and therefore cannot be changed without a change to the high-level mission requirements. With the power being the driving factor in the budgets, the other three must compromise to close all the budgets.

Telemetry RadSat-g telemetry is heavily biased to the housekeeping data. Housekeeping data is the current, voltage, and temperature monitors, as well as status of the processors. The telemetry operation of the RTCS produces a data packet with the fault counts and all RTCS housekeeping, but with a slow cadence of every five minutes. This slow cadence makes for a very small payload telemetry. The entire RTCS data can be reported in a beacon packet and would meet the requirement to have 100% mission success. Empirical data downlink rates from the FIREBIRD missions show the MSU ground-station can downlink approximately 56 Megabytes of data per month during nominal operation. RadSat-g is less than half the maximum downlink rate with the highest RTCS cadences considered. The amount of storage available on the 8 GB NAND memory module allows all data collected during the mission lifetime to be stored. This means, unlike FIREBIRD, RadSat-g does not need to incorporate campaigns that erases stored NAND data.

Communication Link RadSat-g will be deployed from the ISS; therefore, the orbit is well known for the Link Budget parameters. The link budget calculates the received signal strength based off parameters such as effective transmit power, which considers the gain of antennas, path loss, pointing errors, and other factors. This is done for both ground to satellite and satellite to ground communication paths. A good rule of thumb is to have at least 6dB link margin to close the link. Two methods are calculated for determining the link margins and to adequately state the link closes, both methods should be above the 6dB margin.

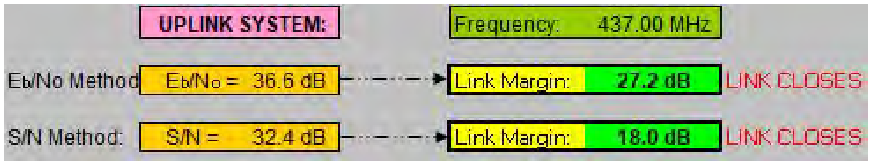
E_BN_O and the S/N Method are the two calculated methods. The E_BN_O uses baud rate and the demodulation method with allowed bit-error-rate to calculate the link margin. From this, the energy of the bit and the noise spectral density can be calculated. The S/N method uses the receiver bandwidth and the calculated noise to calculate the signal to noise ratio [13].

For the RadSat-g satellite with a 1W transmitter and monopole antenna the link is closed with a minimum 7.2 dB margin, see Figure 3.5 and 3.6. The link budget does assume a quasi-symmetrical far-field pattern, so the antenna must be approximately centered to the satellite. This symmetry will add a requirement to the communications and structure subsystems in the RVM.



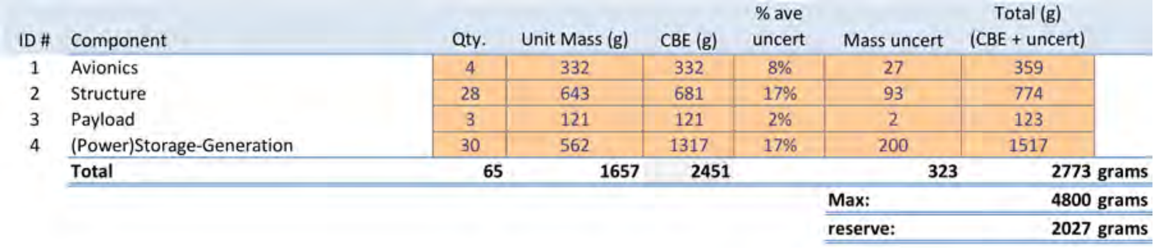
DOWNLINK SYSTEM:
Frequency: 437.00 MHz
Eb/No Method: Eb/No = 19.1 dB → Link Margin: 9.7 dB LINK CLOSES
S/N Method: S/N = 17.2 dB → Link Margin: 7.2 dB LINK CLOSES

Figure 3.5: Down-link Budget



UPLINK SYSTEM:
Frequency: 437.00 MHz
Eb/No Method Eb/No = 36.6 dB → Link Margin: 27.2 dB LINK CLOSES
S/N Method: S/N = 32.4 dB → Link Margin: 18.0 dB LINK CLOSES

Figure 3.6: Up-link Budget

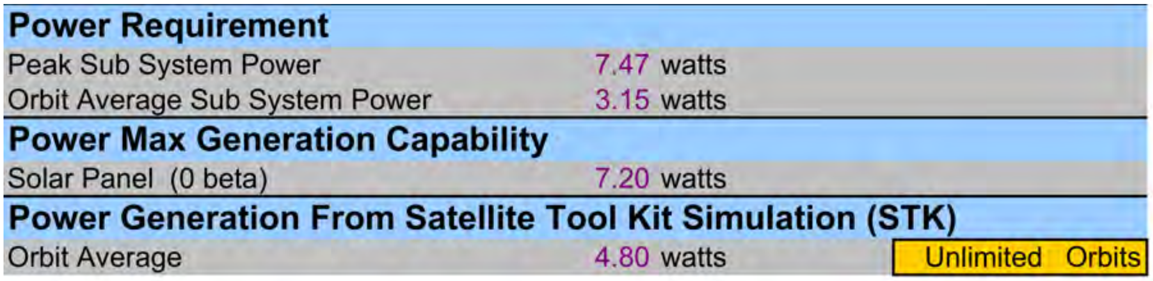


ID #	Component	Qty.	Unit Mass (g)	CBE (g)	% ave uncert	Mass uncert	Total (g) (CBE + uncert)
1	Avionics	4	332	332	8%	27	359
2	Structure	28	643	681	17%	93	774
3	Payload	3	121	121	2%	2	123
4	(Power)Storage-Generation	30	562	1317	17%	200	1517
	Total	**65**	**1657**	**2451**		**323**	**2773 grams**
						Max:	**4800 grams**
						reserve:	**2027 grams**

Figure 3.7: Mass Budget for RadSat-g

Mass The maximum mass of the satellite is dictated by the Launch Service Provider (LSP) and is dependent on the size of the CubeSat. For example, the 3U RadSat-g has a maximum of 4800 g per the NanoRacks Interface Control Document (Change Notice NR-SRD-052). As of September 2017 RadSat-g has a mass measuring 2773 grams, see Figure 3.7, so there is a 42% reserve. Other requirements on the mass properties is the center of gravity, it “shall be within 2 cm of the geometric center” [14]. Ballast is required for RadSat-g to satisfy the NanoRacks center of gravity requirements. If RadSat-g adds additional ballast to reach the maximum weight allowed, the added weight will increase the lifetime of the mission because atmospheric drag force will have to act on a larger mass. The larger mass means less acceleration according to Newtons laws and therefore will de-orbit slower. Having the maximum mass is an advantage for the RadSat-g mission because the longer periods the RTCS can operate in a radiation intensive environment, the more confidence can be obtained in its radiation mitigation technique.

Power The main driver in the budgets is the power budget for RadSat-g. The data for the power budget comes from the Satellite Tool Kit (STK) which is a orbit simulation tool. The first power budget developed used data for direct energy transfer. Using direct energy transfer the power budget did not close. It would have required a power cycling of the RTCS, which is contrary to the M-2 requirement. A 3U panel using the SpectroLab UTJ cells can physically fit 7 solar cells on a side. This would not be amenable for direct energy transfer because it is impossible to balance the strings with an odd number of cells. This forced RadSat-g to develop a power point tracking (PPT) system to remove the requirement of matching the solar panel voltage to the nominal battery voltage. Once the 7th cell was added to the panel, the power budget closed and the RTCS could stay operational 100% of the time, see Figure 3.8. This added a subsystem requirement to the EPS to use a PPT system for power conditioning.



Power Requirement		
Peak Sub System Power	7.47 watts	
Orbit Average Sub System Power	3.15 watts	
Power Max Generation Capability		
Solar Panel (0 beta)	7.20 watts	
Power Generation From Satellite Tool Kit Simulation (STK)		
Orbit Average	4.80 watts	Unlimited Orbits

Figure 3.8: Power Budget for RadSat-g

Once all the four budgets closed, the rest of the subsystem requirements could be updated to accommodate the changes.

Design Flowdown Requirements of EPS

The added requirement derived from the power budget dictated the EPS Requirement to use a PPT System. The EPS requirements have five subsections to them; System Loads (S1.6.1-6), Power Generation/Storage (S1.6.7-11), Power Inhibits (S1.6.12-13), Latch Up Prevention (S1.6.14-15), and Telemetry Gathering (S1.6.16-19), shown in Figure B.2. These governing requirements dictate how to design the system, but do not fully cover all the features of the EPS. For example, the CD&H has a reset line to reset the EPS processor, but it is not spelled out in the EPS requirements. When building the system, changes to the design can go beyond what has been required from the RVM as long as it does not impact the stated requirements.

System Loads System Loads is where the EPS requirements have other subsystem requirements flow in. The CD&H requires two different voltages from three sources. The +3.3 V and +5 V power supplies to the CD&H are needed to be governed by the WDT (S1.6.14), so that the entire system is reset every approximately twelve hours. However, the Real Time Clocks (RTC) +3.3 V supply (S1.6.6) cannot be governed by the WDT and needs to have continuous operation, as the RTCs count the total mission elapsed time and cannot be interrupted. The MFIB also requires the +3.3 V power governed by the WDT as well as the unregulated voltage that is routed to the Antenna Fire (S1.6.5) and the RTCS (S1.6.4). The COMM board also requires the unregulated switchable unregulated voltage.

The one load that does not flow in from the other subsystems is the EPS power. It is a +3.3 V regulator that can supply at least 50 mA and is governed by the WDT. This powers the EPS processor and peripherals for telemetry gathering.

Power Generation/Storage The main change from heritage on RadSat-g is in Power Generation/Storage (S1.6.8). This requires the use of a PPT system making it impossible to re-use the FIREBIRD Phoenix 2.1 EPS, which used direct energy transfer. The other change is the number of cells in the battery pack. Originally FIREBIRD had a 1P2S battery pack, but because of the higher load from the RTCS over the FIREBIRD payload, more capacity is needed for continuous operation during eclipse (S1.6.9). RadSat-g uses a 2P2S configuration to supply the required nominal +7.2 V with 5200 mAh capacity. As with FIREBIRD, the battery packs need protection from over-voltage, under-voltage, and short circuits (S1.6.10). An Electrical Ground Support Equipment requirement (S1.6.11) states the satellite needs to be able to be charged without solar panels and to allow bypassing of the deployment switches for testing on the ground. Normally it is bad practice to have any circuitry that is not necessary for flight on the satellite, so the required circuitry for S1.6.11 is kept to a minimum.

Power Inhibits Power Inhibits is a Launch Service Provider (LSP) requirement. Other than the protection circuitry on the battery, no electrons can flow in the satellite during launch until deployment. Two mechanical footswitches (S1.6.12) are required for redundant inhibits to guarantee the satellite is un-powered during launch. The LSP allowed for a waiver on the third inhibit because RadSat-g battery capacity is not over a minimum threshold. The Remove Before Flight (RBF) switch (S1.6.13) is solely in place for when the satellite is being transported and the foot-switches cannot be easily depressed such as when transporting it to the launcher. This keeps the satellite off and the 45-minute countdown timer that fires the antenna from advancing, a requirement in another section of the RVM.

Latch-Up Prevention A CubeSat is inherently a single string failure device and is in a radiation intensive environment. Radiation can cause a latch up (S1.6.14), which can be cleared by a power cycle. Latch up prevention is implemented using the WDT (S1.6.14), which power-cycles the entire avionics stack every approximately twelve hours. Although the WDT does not just provide latch up prevention, but also helps mitigate a few other failure modes such as if any of the processors receives a SEU or a processor gets in a unknown state.

Telemetry Gathering The State of Health (SOH) of the RadSat-g starts with its power system. Having telemetry of the power system (S1.6.15, S1.6.17-18) gives an immediate snapshot of the battery and system health. If a subsystem is in error, it might be able to be determined by an increased power draw from nominal and corrective action can be taken using telemetry monitors on the CD&H. In addition to immediate data, long term SOH such as battery capacity can be extrapolated after enough data is transmitted to the ground.

The other telemetry point the CD&H uses is the current WDT time (S1.6.16). This allows the CD&H to prepare the memory system for a power cycle. The WDT circuit will output a pulse every approximately forty seconds and once 1023 pulses are counted the WDT circuit holds the satellite power low, minus the RTCS.

Problem Statement

The RadSat-g mission requires a new Electrical Power System that can utilize the 7S1P Clyde Space solar panels. The Phoenix v2.3 EPS must meet all the mission requirements that incorporate and flow down from MO-1 in support of the RTCS. Heritage must be used where possible to minimize the risk to the mission.

THEORY OF A SATELITE ELECTRICAL POWER SYSTEM

The electrical power system manages all the energy transfer in the CubeSat. Solar energy is converted by solar panels and delivered to the EPS, which regulates it into usable voltages for the various subsystems. Phoenix v2.3 uses Fixed Power Point Tracking to utilize the maximum power available from the solar panels. This circuitry needs to compensate not only for the slow sun-eclipse cycles, but the fast cycles due to the satellite rotating about its center of gravity. To compensate for the changing sun incidence on the panel and the non-linearity of the solar panels, sophisticated circuitry is used to keep the panel at a controlled power by providing a virtual load. The virtual load is achieved by high frequency switching in the circuitry, effectively keeping the voltage at the panel constant by varying the current.

Solar Cells

Solar cells convert light energy from the sun or other artificial light source into electrical energy using the photovoltaic effect. When cells are electrically connected in series, they create a string of cells and the voltage is determined by summing up the voltage of each cell. For RadSat-g the panel is a 7S1P configuration, meaning there are 7 cells in series and no parallel strings. A typical 3U solar panel, such as the one for RadSat-g, can be seen in Figure 4.1 [15]. SpectroLabs UTJ solar cells are used on RadSat-g and are 28.3% efficient at 28 ^oC, meaning if you take the energy density of the sun at 1 AU, 1368 $\frac{W}{m^2}$, and have a 1 m^2 UTJ solar cell it would produce a maximum power output of 387 W [16]. On a 3U CubeSat with 7 SpectroLabs UTJ cells there are 0.018634 m^2 of surface area, giving a theoretical maximum of 7.214 W at zero beta angle. The beta angle is the angle between the normal of the solar cell and the light source vector. The beta angle determines the amount of power

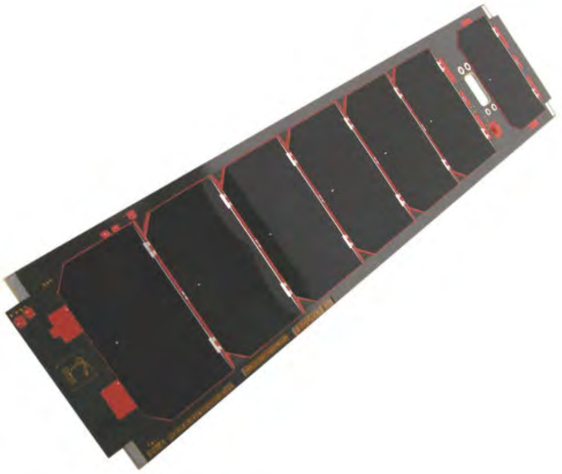


Figure 4.1: Typical 3U Solar Panel

produced due to the cosine dependence on the solar flux incident on the panel. The SpectroLab UTJ cells have a structure of GAlnP$_2$, GaAs, and Ge.

IV Curves

An I-V curve can be empirically found by sweeping the voltage of the panel by using various loads and recording the current produced. When measuring the panel with no load, the V_{OC} or open voltage is the maximum voltage the solar panel can produce. When the output of the solar cell is shorted, the I_{SC} or short circuit current is the maximum current the solar panel can produce. Between these two points is the maximum power, with power being defined as $P = IV$. A typical I-V curve can be seen in Figure 4.2.

To maximize the power produced by a solar cell, the output voltage can be adjusted by changing the load on the cell. To find the maximum power point the derivative of the power vs voltage is set to zero and solved for V. The current of the solar cell follows Equation 4.1, where I_L is the photo-generated current, V_T is the thermal voltage, and I_o is the dark saturation current. Equation 4.1 will produce an

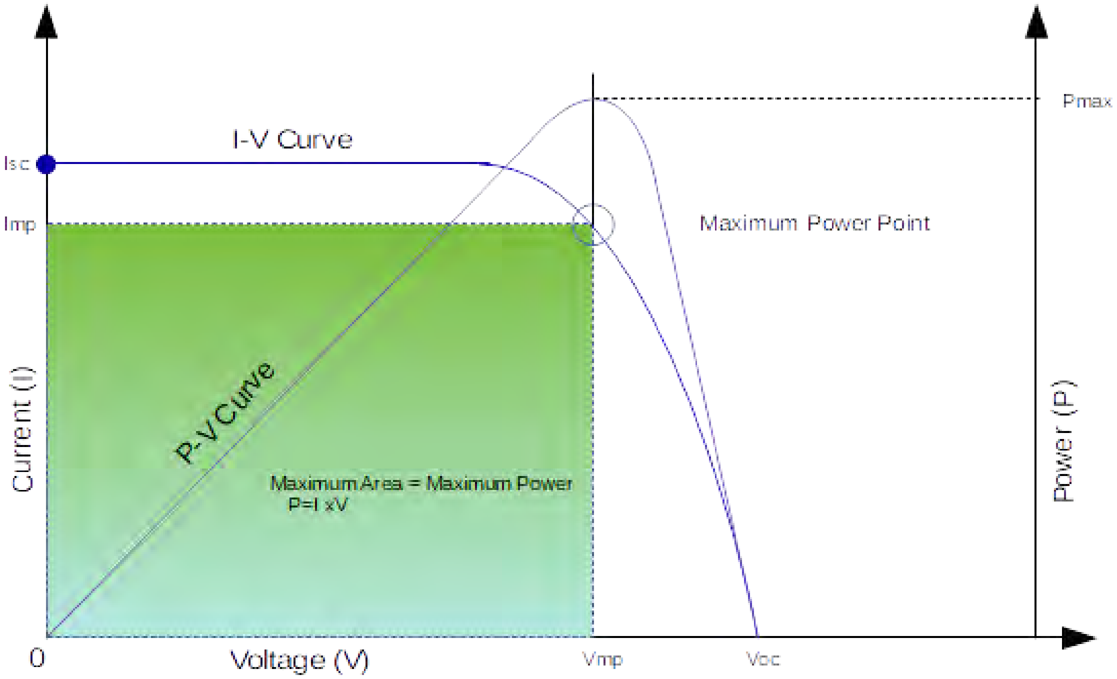


Figure 4.2: Typical I-V Curve

idealized curve such as Figure 4.2. Temperature changes the position of the knee left if the temperature increases and right if the temperature decreases. The amount of solar flux will also vertically shift the entire curve.

$$I = I_L - I_0 \left\{ \exp\left[\frac{V}{nV_T}\right] - 1 \right\} \tag{4.1}$$

Maximum Power Point Tracking

The power available from the solar panel is highly dependent on the voltage set point of the panel. This is why the cells need to be matched to the battery in the case of direct energy transfer, if the battery voltage is too low it will force the power point down the curve, see Figure 4.3, and therefore less power is generated from the panels. The solar cells are matched to the plateau voltage of the battery. This creates an unstable equilibrium in the direct energy transfer power generation, if the battery voltage is high, the power generated also drops off and the battery will settle to a equilibrium. However, if the battery capacity gets to the knee of the battery curve, it will fall off the plateau until it has fully discharged.

Maximum Power Point Tracking (MPPT) fixes this problem as it always sets the voltage to the maximum power point by varying the virtual load the panel sees and can charge the battery to the maximum capacity. For a maximum power tracking system, this is done by a sophisticated hunt and seek algorithm to find the maximum power point. A MPPT system compensates for variables such as panel degradation from radiation and temperature. However, as the beta angle changes from zero to ninety degrees it follows a $cos(\theta)$ drop off, which is not a problem in terrestrial applications where this is caused from the rotation of the earth. This is a slow process, so the MPPT algorithms can easily manage finding the maximum power point without wasting too much time not at the maximum power point. In space when the satellite is tumbling the algorithm may not have time to find the maximum power point because of the rapid changing of the beta angle.

MPPT on a stabilized CubeSat, using an Attitude Determination and Control System (ADCS), can work well due to control of the CubeSat's beta angle. However, on a non-stabilized CubeSat such as RadSat-g, which use passive magnetic attitude control, the rapid beta angle changing nature makes typical MPPT control algorithms unusable.

Fixed Power Point Tracking

The type of power point tracking used by Phoenix v2.3 to mitigate the algorithm problem of MPPT systems is Fixed Power Point Tracking (FPPT). The main difference between FPPT and MPPT, is the FPPT does not seek out the maximum

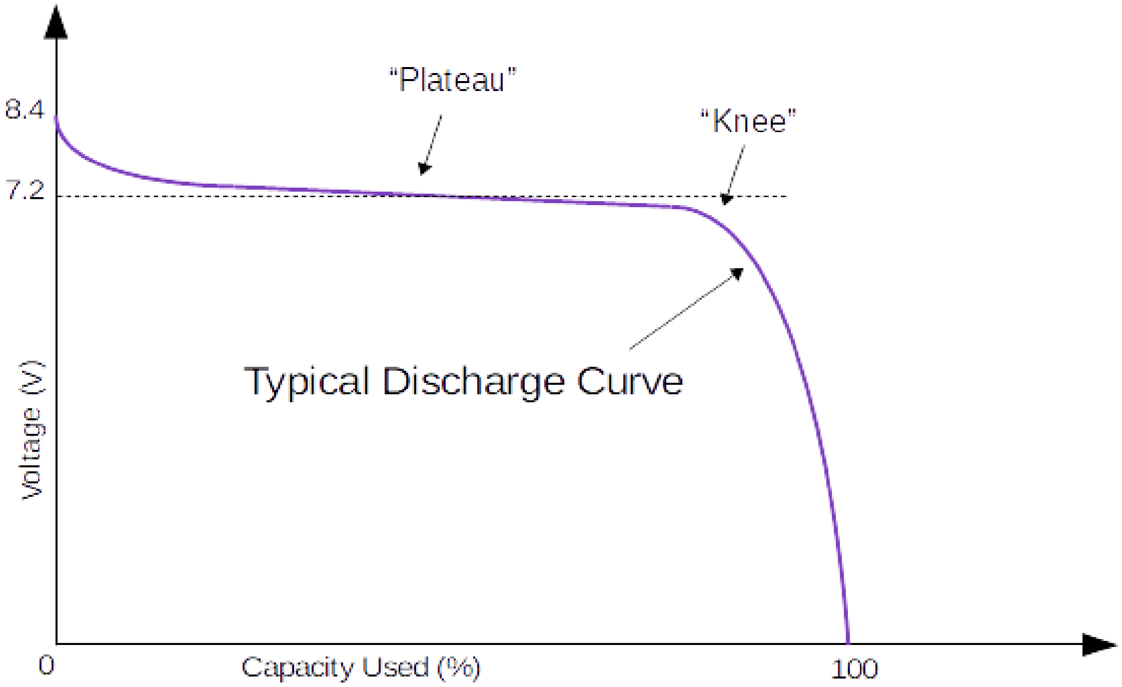


Figure 4.3: Typical Lithium Ion Battery Charge Curve

power point, it uses priori information to set the voltage point to maximize the power. The solar panels for a CubeSat are chosen well before launch and therefore the EPS system can be tailored to the solar panel solution. As stated before, the solar panel's maximum power point also depends on temperature. The satellite experiences large temperatures swings, from -10°C to 40°C , so the voltage set point needs to be also adjusted based on the solar panel temperature. In the operational temperature range the solar panels maximum voltage set point vs. temperature is linear. The SpectroLab UTJ cells have a $-6.5\frac{mV}{°C}$ temperature coefficient, therefore over the expected 50°C range the V_{mp} can change 325 mV. The FPPT uses the same virtual load technique as described above for the MPPT.

FPPT Caculations

The heart of the FPPT is the LT3652 integrated circuit (IC) from Linear Technologies [17]. This charging solution can be used on battery packs up to 14.4 V with a maximum charge current of 2 amps. It can also be parallelized, so is easily expandable for larger solar panel arrays capable of providing more than 2 amps. The RadSat-g solar panels produce less than a half of an amp, so are well within maximum specification.

The LT3652 changes the charge current of the battery to maintain the specified input voltage regulation from the solar panels, effectively having the solar panel see a fixed virtual load. If the battery is fully charged the panel voltage goes to V_{OC} and the solar energy is converted into heat on the panel as no power is extracted from the panel until it is necessary to do so.

The two parameters that are varied on the LT3652 are the input voltage and output voltage. The LT3652 can also modify the battery charge current dependent on temperature, however, the added gain in efficiency did not outweigh the extra complication to the circuitry, which would give another failure mode for the CubeSat. The circuit was designed to be as simple as possible while meeting the requirements of the EPS.

Input Voltage The input voltage loop compensation is achieved using a voltage divider from the input voltage of the solar panel and a temperature dependent current source, shown in Figure 4.4 [17]. For a non-temperature compensated circuit, the LM234 can be removed and the resistors modified.

$$R_{IN1} = -R_{SET} \bullet TC \bullet 4405 \qquad (\Omega) \tag{4.2}$$

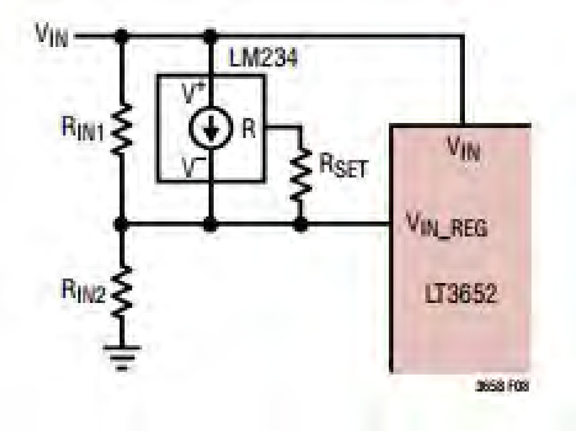


Figure 4.4: FPPT Temperature Compensation Network [17]

$$R_{IN2} = \frac{R_{IN1}}{\dfrac{V_{MP(25°C)} + R_{IN1} \bullet \dfrac{0.0674}{R_{SET}}}{V_{IN_{REG}}} - 1} \quad (\Omega) \tag{4.3}$$

The three resistors R_{IN1}, R_{IN2}, and R_{SET} are chosen with Equations 4.2 and 4.3. The $V_{MP(25°C)}$ is the maximum power at $25°C$, TC is the temperature coefficient from the UTJ SpectroLab Datasheet. $V_{IN_{REG}}$ is +2.7 V from the LT3652 datasheet. The resistor values were calculated using the MATLAB program shown in Appendix C. The three resister values returned by the program can have an order of magnitude change, but the ratio is required to stay the same. The order of magnitude used was chosen to minimize wasted power. These resistors are the highest tolerance components on the EPS. The current source is the LM234, which is a three-terminal adjustable current source with an accuracy of $\pm 3°C$ [18]. The LM234 is required to be thermally mounted on the backside of the panels to obtain the most accurate temperature of the solar cells.

Battery Charge Selection The battery feedback circuit uses a three resister network, shown in Figure 4.5 [17]. Using a three-resister network over a two-resister network makes the resistor selection easier. This is because the V_{FB} requires a 250 kΩ equivalent input resistance. With a three resister selection the battery voltage resistors R_{FB1} and R_{FB2} can be selected without concern for the V_{FB} requirement. After selection of R_{FB1} and R_{FB2}, then the R_{FB3} resistor is selected to compensate by subtracting the parallel equivalents of the battery voltage resistors from 250 kΩ to get the value of R_{FB3}. The three Equations 4.4, 4.5, and 4.6 are used to calculate the resistors, where I_{RBF} is $10\mu A$. The $V_{BAT(FLT)}$ value it is not the nominal battery voltage of +7.2 V, but the maximum battery voltage of +8.4 V.

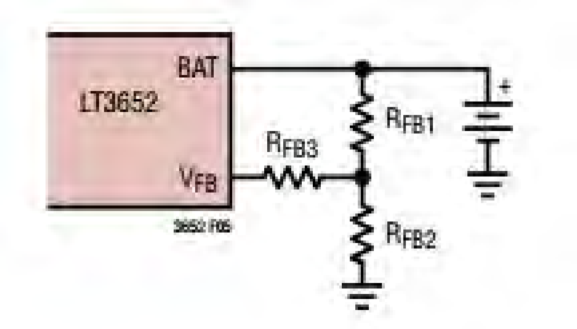


Figure 4.5: Three-Resister Feedback Network for Battery Charging [17]

$$R_{FB1} = \frac{V_{BAT(FLT)} \bullet 2.5 \bullet 10^5}{3.3} \qquad (\Omega) \tag{4.4}$$

$$R_{FB2} = \frac{R_{FB1} \bullet 2.5 \bullet 10^5}{R_{FB1} - 2.5 \bullet 10^5} \qquad (\Omega) \tag{4.5}$$

$$I_{RFB} = \frac{3.3}{R_{FB2}} \qquad (I) \tag{4.6}$$

Inductor Selection

The inductor selection primary changes the ripple current and the efficiency. These two parameters need to be balanced to maintain a stable output voltage and high efficiency of the circuit. The inductor is selected by Equation 4.7. The goal is to have the ripple current within 25% of the $I_{CHG(MAX)}$.

$$L = \frac{\frac{10 \bullet R_{SENSE}}{\triangle I_L}}{I_{CHG(MAX)}} \bullet V_{BAT(FLT)} \bullet \left[1 - \frac{V_{BAT(FLT)}}{V_{IN(MAX)}}\right] \qquad (\mu H) \qquad (4.7)$$

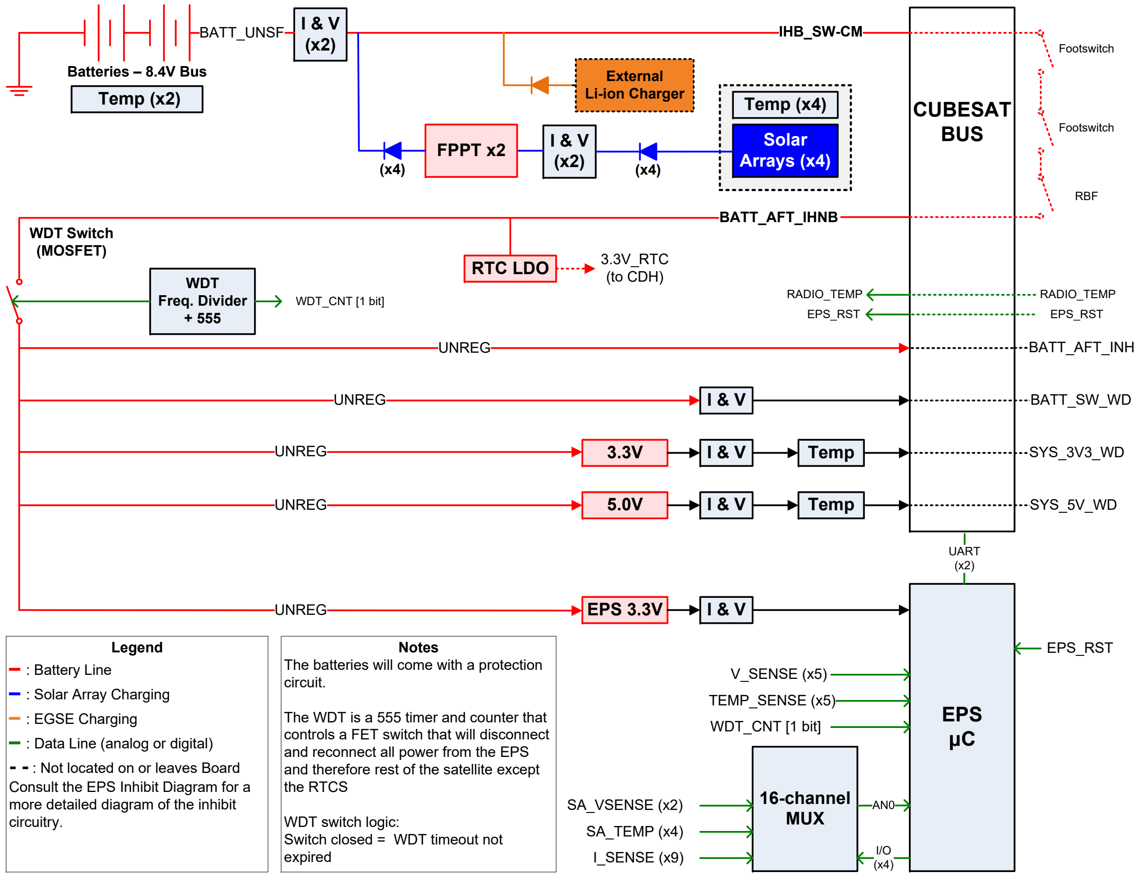
DESIGN OF A SATELLITE ELECTRICAL POWER SYSTEM

The EPS incorporates heritage components from the Phoenix v2.0 board from the FIREBIRD mission as well as new circuity. Per the Problem Statement the EPS must meet all requirements imposed by the flow-down from the MO-1 mission objective. The design will incorporate as much heritage as possible and all new circuity will be fully verified and tested for functionality.

Design of EPS

To capture the requirements for the EPS, a block diagram, shown in Figure 5.1, was first constructed to guide the circuit design. The power flows into the FPPT system after being diode OR'ed with its opposite side panel. The X+ and X- use the same FPPT circuitry because only one side will be illuminated by the sun at a time. Telemetry from the solar inputs will be sent to the EPS micro-controller. The power is conditioned by the FPPT system and charges the battery. Power for the system goes through the three inhibit switches, one remove before flight and two footswitch inhibits. The real time clock regulator, watchdog timer circuit, and the RTCS are connected after the inhibits. The WDT controls the Field Effect Transistor (FET) that supplies power to the rest of the satellite subsystems. Every approximately twelve hours the WDT turns off the FET for ten seconds. After the WDT the unregulated battery voltage lines feed the three regulators on the EPS, two for the system and one for the EPS power as well as the unregulated battery voltage for the radio.

The EPS micro-controller has a 16-channel multiplexer in addition to the 24 analog channels on the PIC processor, which read the telemetry from the power system. Data from the EPS is requested by the CD&H over a UART connection. The EPS micro-controller runs an embedded C program, which once a second gathers


BATT_UNSF
Batteries – 8.4V Bus
Temp (x2)
I & V (x2)
IHB_SW-CM
External Li-ion Charger
CUBESAT BUS
Footswitch
Footswitch
RBF
FPPT x2
I & V (x2)
(x4)
(x4)
Temp (x4)
Solar Arrays (x4)
BATT_AFT_IHNB
WDT Switch (MOSFET)
WDT Freq. Divider + 555
WDT_CNT [1 bit]
RTC LDO
3.3V_RTC (to CDH)
RADIO_TEMP
EPS_RST
RADIO_TEMP
EPS_RST
UNREG
BATT_AFT_INH
UNREG
I & V
BATT_SW_WD
UNREG
3.3V
I & V
Temp
SYS_3V3_WD
UNREG
5.0V
I & V
Temp
SYS_5V_WD
UART (x2)
UNREG
EPS 3.3V
I & V
EPS_RST
V_SENSE (x5)
TEMP_SENSE (x5)
WDT_CNT [1 bit]
EPS µC
SA_VSENSE (x2)
SA_TEMP (x4)
I_SENSE (x9)
16-channel MUX
AN0
I/O (x4)

Legend

— : Battery Line
— : Solar Array Charging
— : EGSE Charging
— : Data Line (analog or digital)
- - : Not located on or leaves Board

Consult the EPS Inhibit Diagram for a more detailed diagram of the inhibit circuitry.

Notes

The batteries will come with a protection circuit.

The WDT is a 555 timer and counter that controls a FET switch that will disconnect and reconnect all power from the EPS and therefore rest of the satellite except the RTCS

WDT switch logic:
Switch closed = WDT timeout not expired

Figure 5.1: Block Diagram of the EPS System

the telemetry. The CD&H requests the telemetry from the EPS every ten seconds, so the power telemetry is at most one second delayed.

Solar Inputs to FPPT Regulators

Each solar panel has a diode on the input to the FPPT system to prevent back feeding from one solar panel to another. All telemetry is read after the diode, so it is not possible to determine which of the two panels, plus or minus, is contributing to the system. This was done for simplification of the EPS system and was heritage on the FIREBIRD mission.

When the battery is fully charged the solar panels will be disconnected from the

Resistor	**Value**	**Tolerance**
R_{IN1}	100KΩ	0.1%
R_{IN2}	17.8KΩ	0.1%
R_{SET}	4.75Ω	0.1%

Table 5.1: Temperature Compensation Resistors

satellite and the voltage will float to the V_{OC}. The input line of the solar panel inputs is voltage divided down so the full scale of the analog inputs of the PIC can read slightly above V_{OC}

In the 7S1P string the maximum current the system can source from the solar panel is 440 mA. To maximize the resolution of the current sense amp, the max current must use the full scale of the PIC analog inputs. The current sense amp has a gain of 100 with a current sense resistor of 60 mΩ, giving a full-scale current of 550 mA. The peripheral components, such as the inductor, were selected to maximize performance with these solar input conditions, not only in power extraction but efficiency of the FPPT system.

Temperature Compensation Calculations Using the equations shown in the Input Voltage section, the resistor values for the temperature compensation network were calculated to be as shown in Table 5.1. Calculations were based using the constants of $-6.5\frac{mV}{^{\circ}C}$ from the SpectroLab UTJ datasheet and V_{MP} of +16.45 V. These resistors have a tolerance of 0.1% as the input voltage is a critical value for obtaining maximum power out of a solar panel.

Battery Connections

The battery compensation network resistors, shown in Table 5.2, used the equations in the Battery Charge Selection section. This assumes a $V_{BAT(FLT)}$ of +8.4 V. The LT3652 can current limit the charge of the battery and is set to 1 A by having the R_{SENSE} set to 100 $m\Omega$. The battery has a capacity of 5200 mAh with an allowable rapid charge current of 0.5 C and the standard charge current of 0.2 C, where C is the capacity of the battery. This gives a standard charge current of 1 A. Setting the current limit is only a precaution as the battery can handle charge current over the max the solar panels can produce [19].

AD590 Temperature Battery temperature is monitored using an AD590 from Analog Devices. The AD590 is a 2-terminal temperature transducer that has a linear current output of $+1\frac{\mu A}{K}$. The AD590 is fed with the WDT unregulated voltage and outputs the temperature dependent current, which is then converted using Ohm's Law by passing the current through a resistor. A value of 4k22Ω is used for the current to voltage conversion. A nominal voltage output at 20 $°C$ is +1.23 V, which is then read by an analog channel on the PIC. This resister selection encompasses the expected temperature range of the satellite with margin.

A change from heritage is how the temperature sensors are physically routed to

Resistor	**Value**	**Tolerance**
R_{FB1}	510kΩ	1%
R_{RB2}	330kΩ	1%
R_{RB3}	50kΩ	1%

Table 5.2: Battery Voltage Network Resistors

the battery. Originally the temperature sensors were a separate connection on the EPS from the battery harness. Now the battery connector is an 8 pin Harwin. This allows for dual redundant power and ground as well as the two temperature sensors to be run in the same harness. This change allows for easier integration into the chassis for final assembly.

Watchdog Circuit

The Watch Dog Timer circuit is heritage from the FIREBIRD mission and has been operating in orbit for over two years. Ground operations have confirmed the WDT circuit has recovered the FIREBIRD satellites numerous times. The WDT circuit uses heritage 4000 series logic IC's. The heart of the WDT is a Texas Instruments CD4060B, a CMOS 14-stage ripple-carry binary counter/divider and oscillator. The period of the pulses sent to the EPS PIC is approximately 40 seconds and the counter pulses a 555 Timer running in Mono-Stable Mode after 1023 ticks. The 555 Timer holds the main FET off for 10.406 seconds to allow all capacitors to fully discharge before re-powering the spacecraft.

Heritage Regulators

All the voltage regulators are also heritage with some layout changes recommended by the previous engineer and the datasheet. The main +5 V and +3.3 V regulator is an LTC3626 Regulator by Linear Technologies. It is a variable buck switching regulator running in Burst Mode as opposed to Forced Continuous Mode. The design decision to run in Burst Mode is based on power conservation. At low currents, which the CD&H and the MFIB draw in normal operation is less than 100 mA. At the current draw of these subsystems the efficiency in Burst Mode is over 90% while the Forced Continuous Mode ranges from 30 to 70%, shown in Figure 5.2 [20]. This regulator is designed to output 2.5 A, so this application is an under-utilization of the regulator. The Burst Mode does add noise to the system, however, RadSat-g is not acquiring any sensitive analog reading so the tradeoff of the gain in efficiency to noise was acceptable. The regulator uses the current limit line to also output the current of the regulator. If the full 2.5 A is necessary it reduces the resolution to 10 mA per ADC count, however having the regulator current limited at 0.5 A, which is more than capable of handling the load expected, the resolution is approximately 2.5 mA.

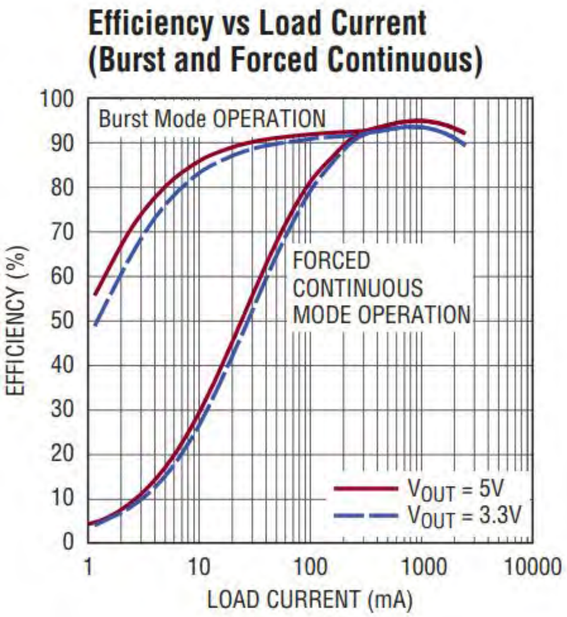


Figure 5.2: LT3626 Efficiency of Regulators [20]

The +3.3 V regulator for the EPS is a LTC3642 from Linear Technology and is also a buck switching regulator, but can only source 50 mA for the load. With the current draw of the EPS, the regulator runs at an efficiency above 93% [21]. This regulator could not be an option for the other +5 V and +3.3 V requirements because it could not handle the demand from the CD&H and MFIB.

The last regulator on the EPS board is the Real Time Clock regulator. This is required because of the LSP requirements. The CD&H from Pumpkin has a button cell battery to run the RTC, however this would violate the LSP requirement of no current flowing before deployment. Instead, the RTC uses a LT3008 LDO Linear Regulator from Linear Technology. The regulator can supply a max of 20mA, which is more than enough to run the RTC on the CD&H [22]. The regulator output line is attached to the positive side of the button cell battery terminal on the CD&H via a wire jumper. The RTC will run continuously once the foot-switches deploy and cannot be shutoff.

The main layout changes made were to follow the datasheets suggestion on the inductor and capacitor placement to reduce noise on the output line.

HARDWARE FABRICATION

After the high level design was completed the Electrical Interface Control Document for the pin-out of RadSat-g, Figure A.1, was constructed based off the CD&H pins that were already defined by Pumpkin. The other pins, which were no-connects on the CD&H, were available for use between the Radio, MFIB, and EPS. The MFIB and Radio boards were not designed at the time the EPS was being built, so the foreseen pins needed to be allocated to the pin-out document to ensure adequate availability for the other subsystems. Once these two documents were in place, the schematic of the EPS was created.

Schematic

The program used for schematic capture was XDxDesigner. This program was already in use in the Electrical Engineering Department and had some ability to import parts already created for the Phoenix v2.1 board. Each part in the library had to be updated to correctly transfer to the layout program. An example of the schematic layout of the FFPT circuity can be seen in Figure 6.1.

Each part has a symbol and a physical decal with META data associated with it such as the manufacture, manufacture part number, voltage tolerances, and other such useful information. Once these symbols were designed, they are placed in the schematic editor. The lines connecting two symbols are called nets and are representative of physical electrical connections between terminals. Each net has a unique name for easy troubleshooting and off page connections such as the flag SA_Y_Raw. The thick lines are BUS lines with multiple nets associated with them and are used for easy reading of the schematic.

The entire document is divided into eight pages each organized with similar sub circuitry; BUS_INTERFACE, SOLAR_ARRAYS, BOOST, BATTERY_CHARGE, REGULATORS, WATCHDOG, TLM_COLLECTION, and MICROPROCESSOR. Figure 6.1 is a sub section of the page labeled BOOST.

Once each sub circuit was completed the error checking tool was run to determine if there was any unconnected nets or pins. Then once the entire schematic was finished the tool was executed again and any errors were fixed before moving to the layout portion of the hardware fabrication.

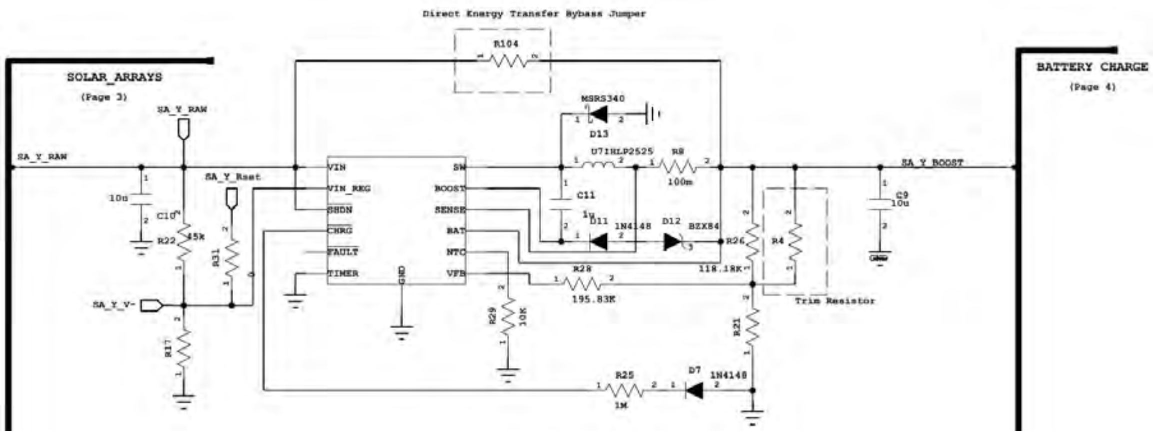

Direct Energy Transfer Bybass Jumper
R104
SOLAR_ARRAYS
(Page 3)
SA_Y_RAW
SA_Y_RAW
SA_Y_Rset
10u
C10
R22
45k
R31
SA_Y_V-
R17
VIN
VIN_REG
SHDN
CHRG
FAULT
TIMER
GND
SW
BOOST
SENSE
BAT
NTC
VFB
R29
10K
MSRS340
D13
U7IHLP2525
R8
100m
C11
1u
D11
1N4148
D12
BZX84
R26
118.18K
R4
R28
195.83K
Trim Resistor
R21
R25
1M
D7
1N4148
SA_Y_BOOST
C9
10u
BATTERY CHARGE
(Page 4)

Figure 6.1: FPPT Schematic for RadSat-g

Layout

The layout was performed in another program called PADS. Once the link between the two programs was established, the physical footprints of the parts and all associated net connections were placed in the layout window. Each footprint was verified and fixed if needed. The outline of the board, mounting holes, and 104 pin headers were first placed. These were dictated by the avionics stack to insure interconnection between subsystems and harnessing paths.

For the Phoenix v2.3 EPS a total of four layers were chosen to keep production cost at a minimum. The two outside layers are component layers while the two inner layers were a ground plane and signal layer. The board was also divided into an analog side and a digital side. The analog side had the regulators, FPPT circuity, and telemetry gathering. While the digital side had the PIC microprocessor, MUX, and the WDT circuitry. The two sides are separated by a copper ground plane to assist in mitigating noise. Each net translated from the schematic, called an airwire, was replaced with a copper trace. The trace width calculator was used to ensure the trace width were the appropriate for the expected amount of current. Signal traces were 8 mils (1 mil = 0.001") and power traces were up to 50 mils in width. Inner layer connections used a vertical interconnect access (VIA), which is a copper barrel that spanned all four layers.

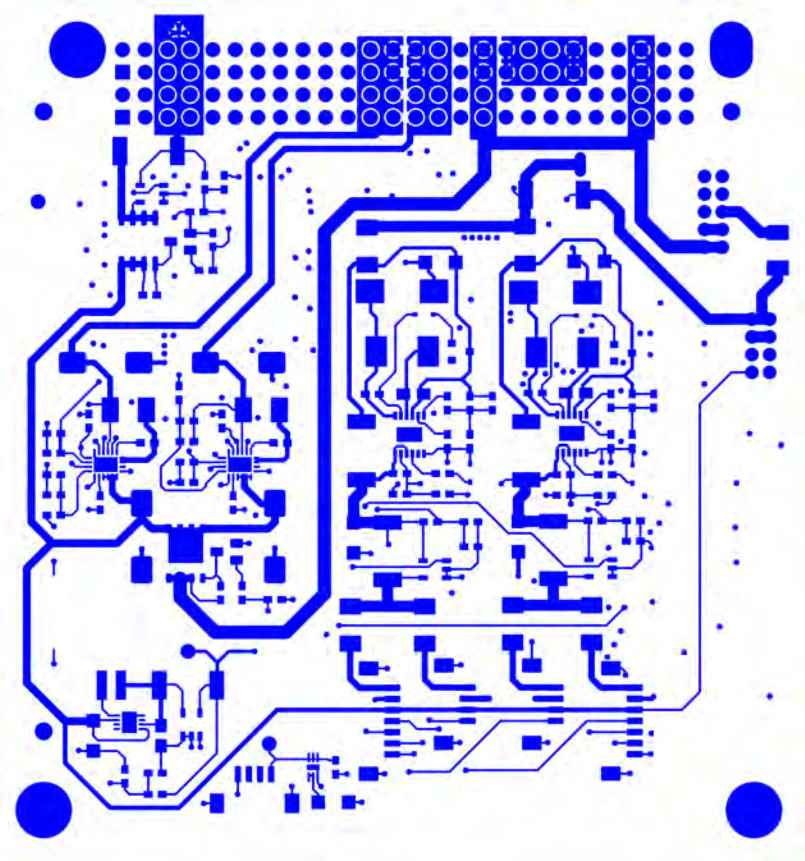


Figure 6.2: Bottom Side Layout for RadSat-g

After the layout was complete the Design Rule Check (DRC) tool was used to find any missing electrical connection and check tolerances between traces. The specification the DRC used were provided from the chosen manufacture of the EPS board, Advanced Circuits. Once complete, the Computer-Aided Manufacturing (CAM) files were created for the fabrication at Advanced Circuits. An example of one of the component level CAM files is shown in Figure 6.2. The Intermediate Data Format (IDF) files were also exported from PADS to assist in creating the SolidWorks model such as the one in Figure 3.2.

Fabrication

Once the CAM files for the Phoenix v2.3 EPS were sent to Advanced Circuits, which provided a second DRC. This is a more complete DRC then the ones used to verify the design. Once the DRC from Advanced Circuits was are completed, the EPS board was submitted for fabrication. Advanced Circuits offers a discount for four layered boards with no minimum order for students. This is the main reason why restricting the layout to four layers were chosen. If, for example, it was a six layer board the fabrication would cost closer to a thousand dollars. Once the boards were returned a visual inspection was performed. This looks for defects such as lifted pads or incorrect masking. An example of the blank fabricated EPS board can be seen in Figure 6.3.

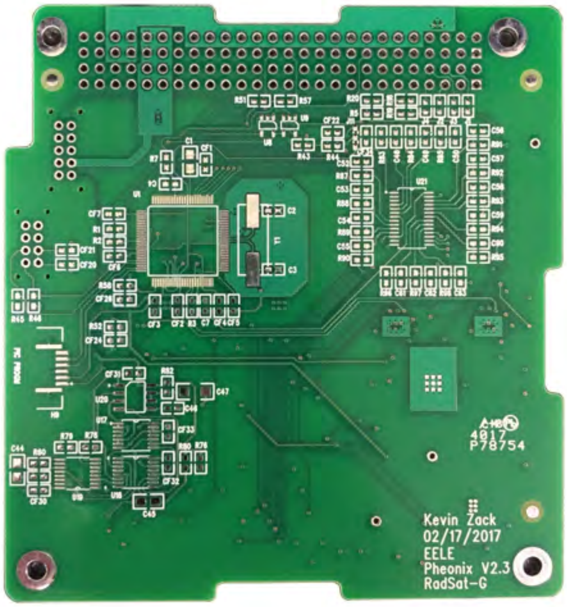


Figure 6.3: Blank EPS Board

Assembly

During the fabrication time the bill of materials was ordered and the assembly guide was created. Figure D.1 is an excerpt of one page out of the assembly guide document. This document spells out the assembly instructions for the Phoenix v2.3 EPS. Each part is listed, as well as its Reference Designator and any no-loads on the board to inform the builder how to load the parts. The board has options such as the communication path to change which UART to use for flexibility in software. The fully assembled top side of the EPS board is shown in Figure 6.4, and the bottom is shown in Figure 6.5. Once the board was assembled, a thorough cleaning and visual inspection was performed. This can find errors in part placement before moving on to Safe to Mate (STM) verification.

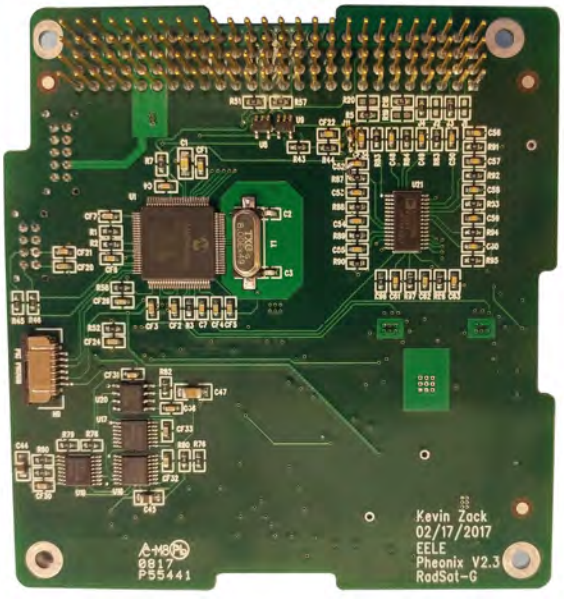


Figure 6.4: Top Side Assembled Board

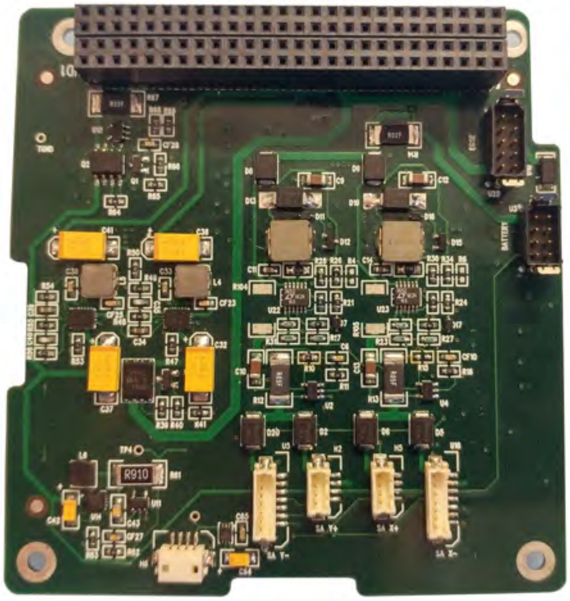


Figure 6.5: Bottom Side Assembled Board

ANALYSIS

All avionics section subsystem boards go through a rigorous acceptance testing before use in the satellite. The testing starts at the board level and then completes when the stack is fully integrated.

Analysis Of EPS

Once the EPS is fully assembled each component is examined under the microscope to verify all parts are properly soldered and to verify there is no solder bridges or degradation of components. The EPS then go through a Safe to Mate process. This is a documented procedure that verifies functionality before integration with other subsystems in the stack. Once the STM passes, the next step is a functional test to fully exercise every part of the sub circuity on the board.

Safe To Mate

The STM has two purposes, the first is to verify the assembly of the board, and to give a baseline for future analysis. If the board later has a malfunction and troubleshooting is required, having a known state to compare against expedites the process.

There are two parts to a STM. The first is an unpowered test such as the excerpt shown in Figure D.2, that measures the ohm value of each pin referenced to ground. All the off-board connections including the grounding mounting points of connectors and select test points are also measured. From analysis of the circuity the expected values for each pin/test point is approximated before the test. For example, in Figure D.2, Pin 1 in HD1 is the EPS_RST pin. From the analysis of the schematic it was determined the resistance to ground reading should be approximately 117kΩ.

If the resistances measured is not within tolerances for this pin the STM fails and the problem is investigated. The first STM of a production run is the most difficult because the expected resistances are educated guesses. Once a board successfully passes the STM procedure, the document is then updated to the accepted resistance values for testing future boards. The first successful STM is the baseline for all future STM. The purpose of the unpowered STM is to ensure when the board is powered for the first time it does not damage itself.

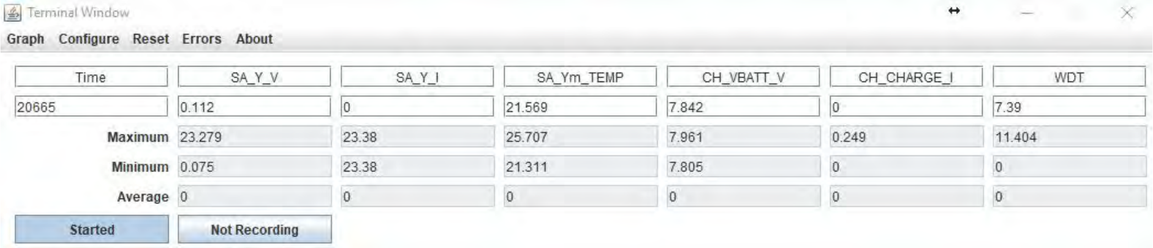
The powered STM test is to make sure the board does not damage any other boards it is mated into. The powered STM uses the expected voltage referenced to ground. One thing to note is for communication lines there is a difference in both the unpowered and powered part of the STM before and after the PIC is programmed. Once the board passes its powered STM it is ready to be programmed and integrated into the stack. A STM that has passed is stated to be an As-Run, and is scanned into the document control system.

Functional Testing

When the EPS is ready to be integrated into the rest of the stack the board starts its functional testing. Every subcircuit needs to be exercised, meaning the full program chain from EPS to ground station must be complete to finish the functional testing. The first task is to program each PIC processor in the system. The tools with the ICD 3 programming puck used by MPLab, the Integrated Development Environment, verifies the connection and the memory blocks to be programmed.

For this stage of the functional test, the EPS was integrated with the CD&H and the Ground-station Support Equipment (GSE). The GSE is used for the communication link between RadSat-g and the ground software, InControl. InControl is the mission support software that facilitates the command and telemetry gathering for the mission. To properly preform a functional test, the code in the EPS, CD&H, and InControl all must be working flawlessly for the information to be transferred. During the functional test of the EPS each command was executed and verified.

After the functional test was completed the EPS was removed from the stack for "test only" configuration that automatically executed the telemetry gathering command to remove the need for the CD&H and InControl. This facilitated verification of the FPPT circuitry by sending the telemetry packet out the UART once a second. The data was sent to the DataLoger program written specifically for this EPS, shown in Figure 7.1. This program was written in Java and had the ability to store all telemetry points as well as graph any data point against any other. It could also do basic arithmetic, so two points such as panel voltage and current could be multiplied together to create a power data point and graphed against time.



Time	SA_Y_V	SA_Y_I	SA_Ym_TEMP	CH_VBATT_V	CH_CHARGE_I	WDT
20665	0.112	0	21.569	7.842	0	7.39
Maximum	23.279	23.38	25.707	7.961	0.249	11.404
Minimum	0.075	23.38	21.311	7.805	0	0
Average	0	0	0	0	0	0

Figure 7.1: DataLogger Program

The data from the DataLogger program verified each telemetry point was working such as current, voltage, and temperature of each regulator and battery as the FPPT testing was underway. The DataLogger also verified the WDT functionality in the long-term testing phase. During the temperature compensation testing it was used as a secondary verification of voltage and current compared against the Agilent 34410A digital multimeter that was connected.

Temperature Compensation Test

Verification of the temperature compensation circuit was performed in the Tenney T10S-1.5 Environmental Test Chamber in the SSEL Lab. This is an active temperature controlled environmental chamber that has a range beyond the expected temperatures the satellite will experience in orbit. The EPS board with a temperature sensor and the temperature compensation component, LM234, was placed in the environmental chamber with leads leaving a pass-through port to the solar panel. A light source directed at a test solar panel provided the source for the solar panel inputs. The solar panel was connected in parallel to one Agilent multimeter and in series with another Agilent multimeter. This allowed for both voltage and current of the panel to be measured at a high cadence.

The first experiment started with a stabilized temperature of $60°C$ and then the environmental chamber was commanded to -5 $°C$. The voltage responded to the change in temperature appropriately and the nonlinear change of the environmental chamber can be seen in the curve in Figure 7.2. This was the first verification of the temperature compensation circuit as it showed it had the correct sign on the TC value.

The following experiment verified the actual linearity of the system and the TC coefficient. The environmental chamber started at $-5°C$ and each $5°C$ step was allowed to stabilize for a minimum of five minutes. Now the solar panel was illuminated and a minimum of sixty seconds of data was collected, which resulted in over 5500 data points collected from the Agilent 34410A digital multimeter. The data points were averaged for each datapoint and the standard deviation was calculated for the error bars. This was repeated until the chamber temperature reached $60°C$. The resultant graph is shown in Figure 7.3. The line of best fit gave a coefficient of -6.24 V/K compared to the expected -6.5 V/K. This gives an error of only four percent, well

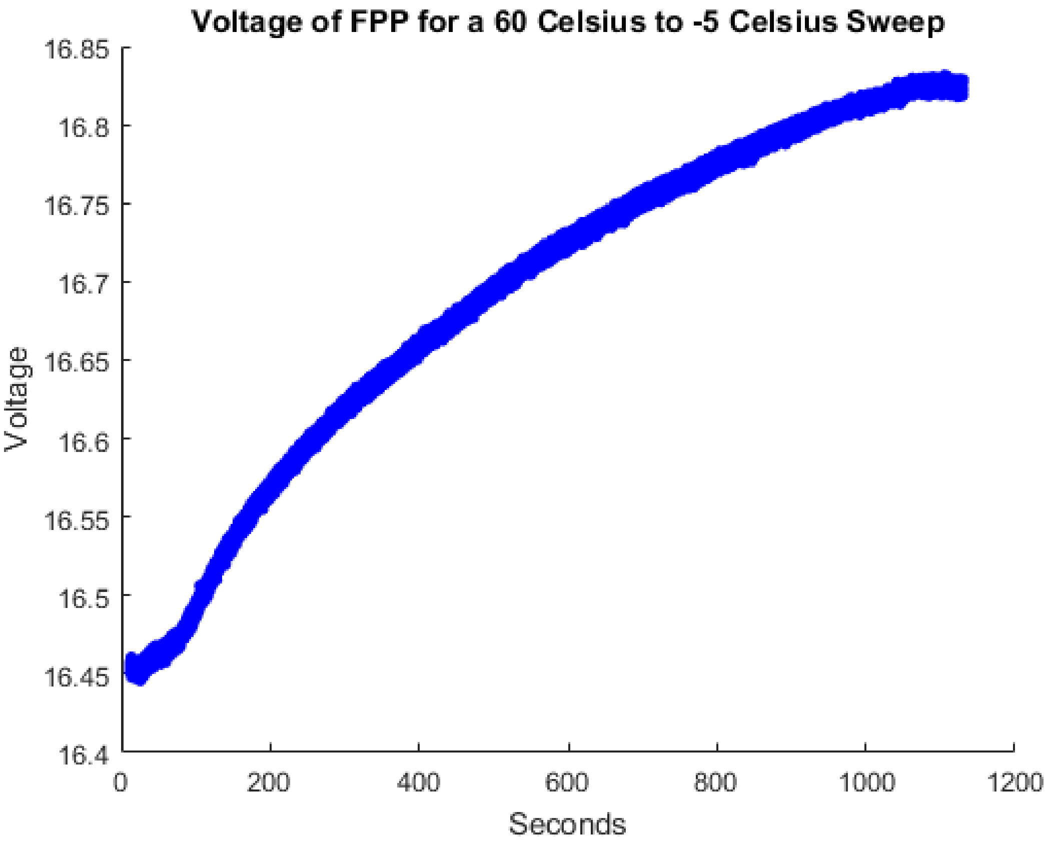


Figure 7.2: V_{MP} sweep of temperature

within acceptable tolerances for this parameter given the environmental chamber could only maintain a $\pm 2°C$ temperature.

Response of FPPT Circuitry

The prior analysis verified the temperature compensation, however part of the main problem with power point trackers is the response to the rapid beta angle changes. To test this a rotating platform with a slip ring to allow for power transfer was designed and built, shown in Figure 7.4. The platform has a variable rotation rate using a stepper motor, so different response curves could be obtained. The simulated light source is a halogen lamp.

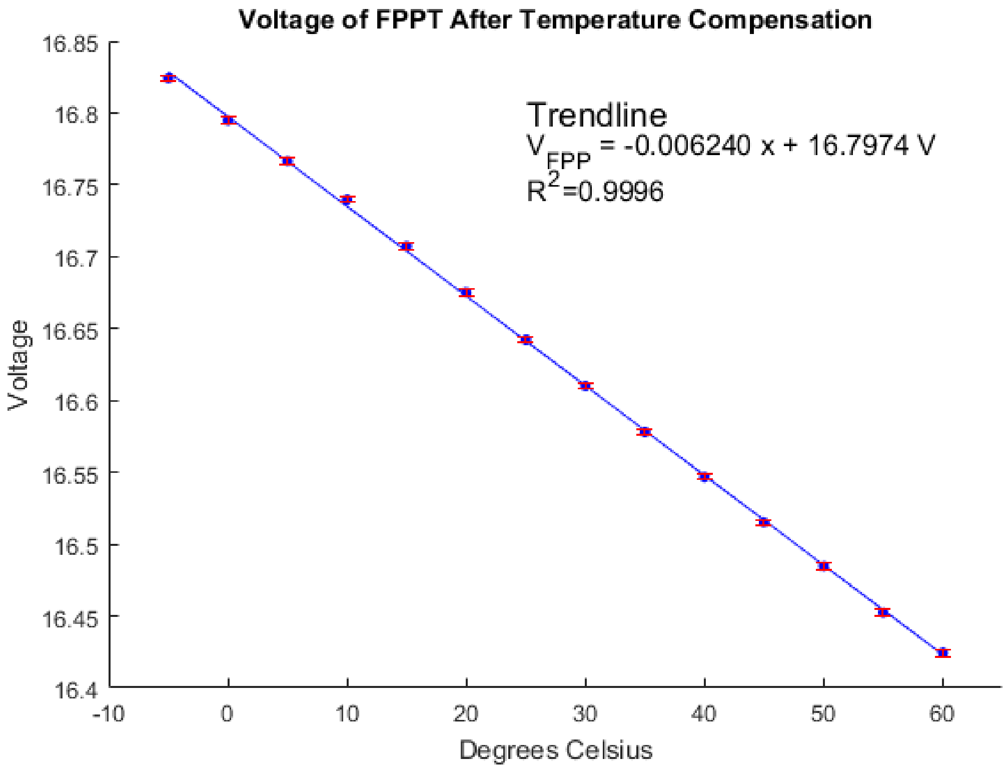


Figure 7.3: V_{MP} based off Temperature

The same Agilent 34410A digital multimeter setup for the temperature compensation measurements was used taking a sample every 6 ms. With the solar panel spinning at a rate of 1.11 radians per second the current was measured, which is a function of light flux and dependent on $cos(\beta)$. The overlaid cos function and raw data can be seen in Figure 7.5. The system starts to produce current into the battery at 87° beta angle. A fast spin at a rate of 3.7 radians per second of the solar panels are shown in Figure 7.6. The system responded correctly for each of these spin rates, proving the problem with the search algorithm style MPPT is not a factor when using the FPPT.

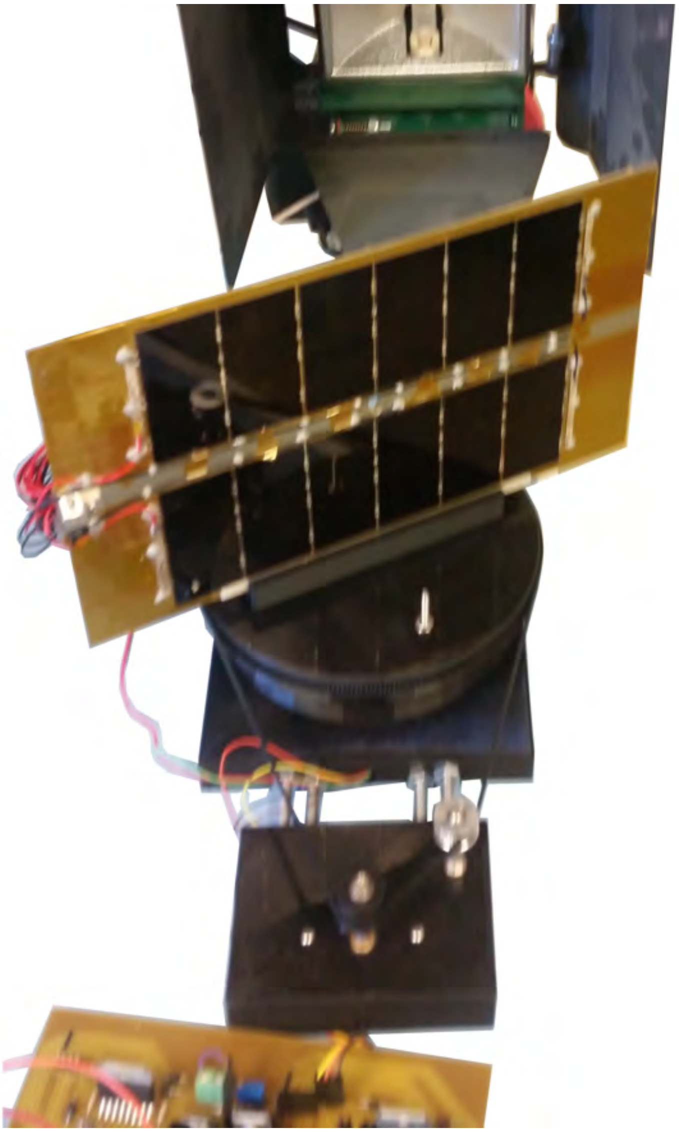


Figure 7.4: Setup of spinning solar panel

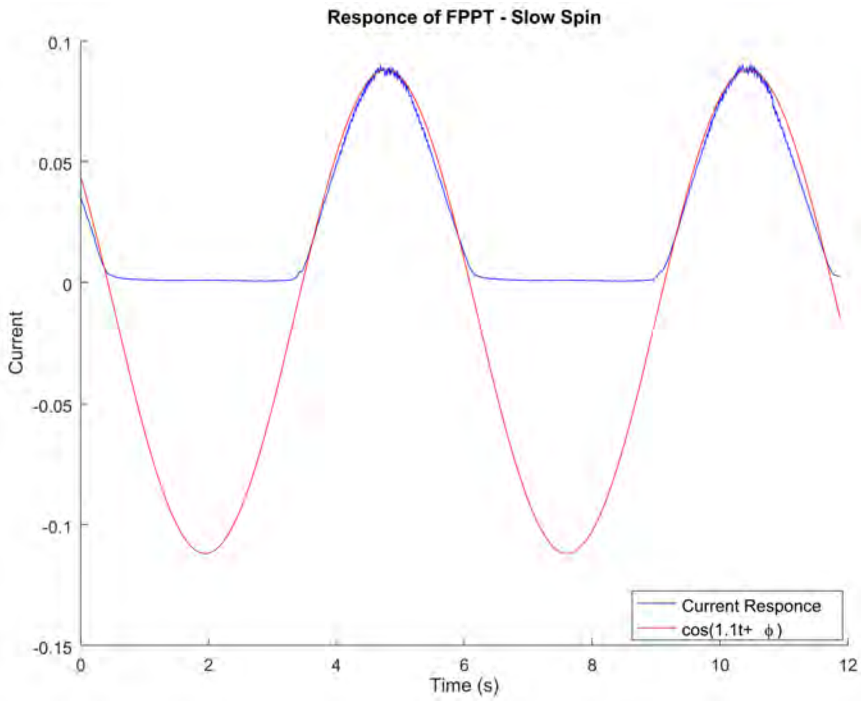


Figure 7.5: Voltage Response - Slow Spin of Solar Panel

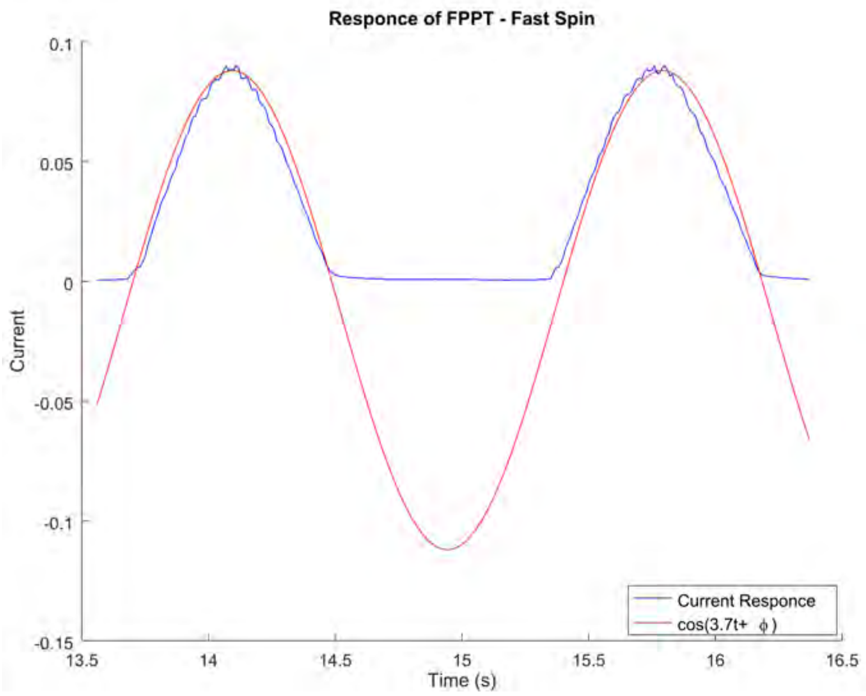


Figure 7.6: Voltage Response - Fast Spin of Solar Panel

CONCLUSION

The Phoenix v2.3 EPS passed all the testing and preforms as intended. It meets all the flowdown requirements from the mission objective. The EPS has been operating with the CD&H for long term testing and the RadSat-g mission has begun full stack integration.

Leasons Learned

The solar panels were ordered before finalization of the EPS. This meant the solar panels do not come with the required temperature compensation sensor. While there is a work around for getting the sensor on the solar panels, it would have been better if more time was spent thinking about the interconnection between the EPS and the solar panels. The temperature sensors and temperature compensation network could have been part of the solar panel design, so a simple harness could connect the two. The workaround is a daughterboard that houses the temperature compensation sensor and the AD590 temperature sensor that will be bonded to the back of the solar panel before integration.

The Harwin connectors for the umbilical and battery harness are a vertical latching type connector and should have been the more robust jackpost style. The latches have a low duty cycles, so care must be taken to avoid breaking the tabs. Also, the Harwin connector should have also been a right-angle connector as to leave the EPS board horizontally. Currently a double header is necessary to maintain proper bend radius from the vertical connectors.

Future Recommendation

If the EPS was to be redesigned a few changes should be made. The first is each panel should have its own FPPT tracking. The heritage design diode OR'ed the X+ and X- panel together as well as the Y+ and Y- panels. This logic was because if the panel was illuminated by the sun then the other panel would be opposite of the sun and therefore would not produce power. However, sunlight reflected off the earth can produce a small amount of power, which will add up over the mission lifetime. With a FPPT system for each panel it would be able to extract out the low amount of light reflected from the planet. This change would also allow for independent telemetry for each solar panel.

Not just for the EPS, but all boards, the PIC processor should be able to be programmed through the umbilical like IT-SPINS mission can. This enables more parallel work to be done, as you can assemble the avionics stack in the chassis and still program the processors.

Finally, the regulators should be reworked to reduce noise. If the load is over 200 mA then the current LT3652 regulators should be operated in Forced Continuous mode to reduce noise on the system. If the load is less than 200 mA, the LT3652 regulator should feed a new LDO regulator at a voltage slightly above its dropout to keep efficiency high. This switching regulator feeding an LDO configuration reduces noise and keeps efficiency high.

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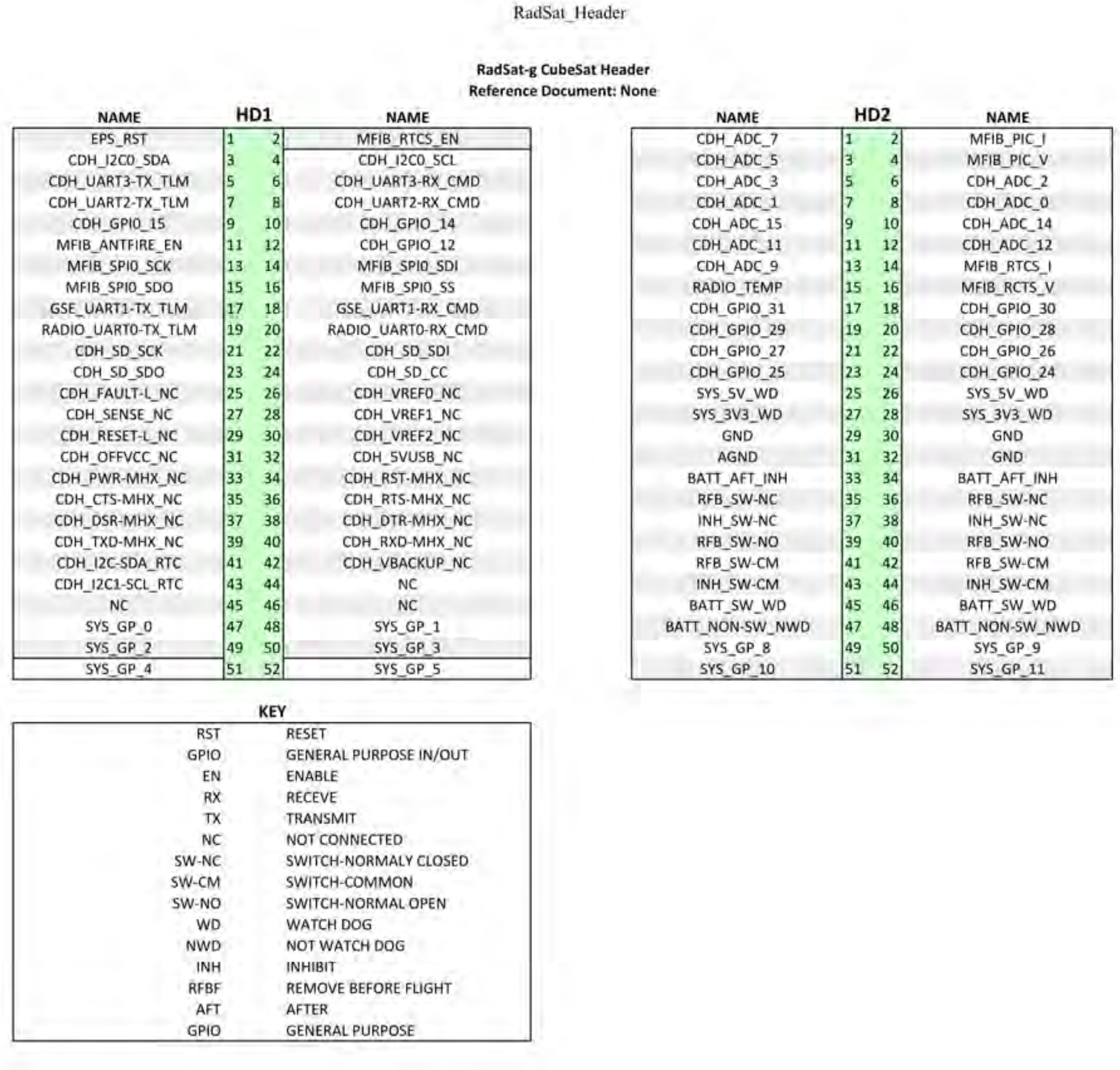
APPENDICES

APPENDIX A

DIAGRAMS



RadSat_Header

RadSat-g CubeSat Header
Reference Document: None

NAME	HD1		NAME
EPS_RST	1	2	MFIB_RTCS_EN
CDH_I2C0_SDA	3	4	CDH_I2C0_SCL
CDH_UART3-TX_TLM	5	6	CDH_UART3-RX_CMD
CDH_UART2-TX_TLM	7	8	CDH_UART2-RX_CMD
CDH_GPI0_15	9	10	CDH_GPIO_14
MFIB_ANTFIRE_EN	11	12	CDH_GPIO_12
MFIB_SPI0_SCK	13	14	MFIB_SPI0_SDI
MFIB_SPI0_SDO	15	16	MFIB_SPI0_SS
GSE_UART1-TX_TLM	17	18	GSE_UART1-RX_CMD
RADIO_UART0-TX_TLM	19	20	RADIO_UART0-RX_CMD
CDH_SD_SCK	21	22	CDH_SD_SDI
CDH_SD_SDO	23	24	CDH_SD_CC
CDH_FAULT-L_NC	25	26	CDH_VREF0_NC
CDH_SENSE_NC	27	28	CDH_VREF1_NC
CDH_RESET-L_NC	29	30	CDH_VREF2_NC
CDH_OFFVCC_NC	31	32	CDH_5VUSB_NC
CDH_PWR-MHX_NC	33	34	CDH_RST-MHX_NC
CDH_CTS-MHX_NC	35	36	CDH_RTS-MHX_NC
CDH_DSR-MHX_NC	37	38	CDH_DTR-MHX_NC
CDH_TXD-MHX_NC	39	40	CDH_RXD-MHX_NC
CDH_I2C-SDA_RTC	41	42	CDH_VBACKUP_NC
CDH_I2C1-SCL_RTC	43	44	NC
NC	45	46	NC
SYS_GP_0	47	48	SYS_GP_1
SYS_GP_2	49	50	SYS_GP_3
SYS_GP_4	51	52	SYS_GP_5

NAME	HD2		NAME
CDH_ADC_7	1	2	MFIB_PIC_I
CDH_ADC_5	3	4	MFIB_PIC_V
CDH_ADC_3	5	6	CDH_ADC_2
CDH_ADC_1	7	8	CDH_ADC_0
CDH_ADC_15	9	10	CDH_ADC_14
CDH_ADC_11	11	12	CDH_ADC_12
CDH_ADC_9	13	14	MFIB_RTCS_I
RADIO_TEMP	15	16	MFIB_RCTS_V
CDH_GPIO_31	17	18	CDH_GPIO_30
CDH_GPIO_29	19	20	CDH_GPIO_28
CDH_GPIO_27	21	22	CDH_GPIO_26
CDH_GPIO_25	23	24	CDH_GPIO_24
SYS_5V_WD	25	26	SYS_5V_WD
SYS_3V3_WD	27	28	SYS_3V3_WD
GND	29	30	GND
AGND	31	32	GND
BATT_AFT_INH	33	34	BATT_AFT_INH
RFB_SW-NC	35	36	RFB_SW-NC
INH_SW-NC	37	38	INH_SW-NC
RFB_SW-NO	39	40	RFB_SW-NO
RFB_SW-CM	41	42	RFB_SW-CM
INH_SW-CM	43	44	INH_SW-CM
BATT_SW_WD	45	46	BATT_SW_WD
BATT_NON-SW_NWD	47	48	BATT_NON-SW_NWD
SYS_GP_8	49	50	SYS_GP_9
SYS_GP_10	51	52	SYS_GP_11

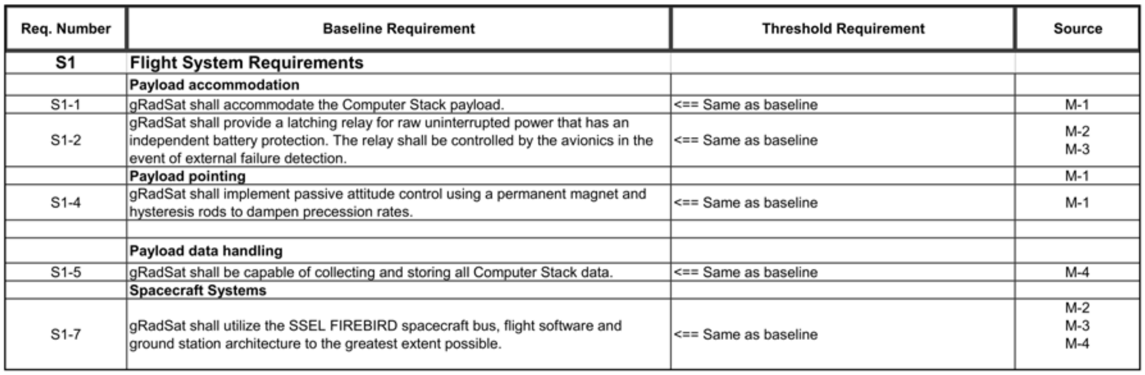
KEY

RST	RESET
GPIO	GENERAL PURPOSE IN/OUT
EN	ENABLE
RX	RECEVE
TX	TRANSMIT
NC	NOT CONNECTED
SW-NC	SWITCH-NORMALY CLOSED
SW-CM	SWITCH-COMMON
SW-NO	SWITCH-NORMAL OPEN
WD	WATCH DOG
NWD	NOT WATCH DOG
INH	INHIBIT
RFBF	REMOVE BEFORE FLIGHT
AFT	AFTER
GPIO	GENERAL PURPOSE

Figure A.1: CubeSat Header Pinout for RadSat-g

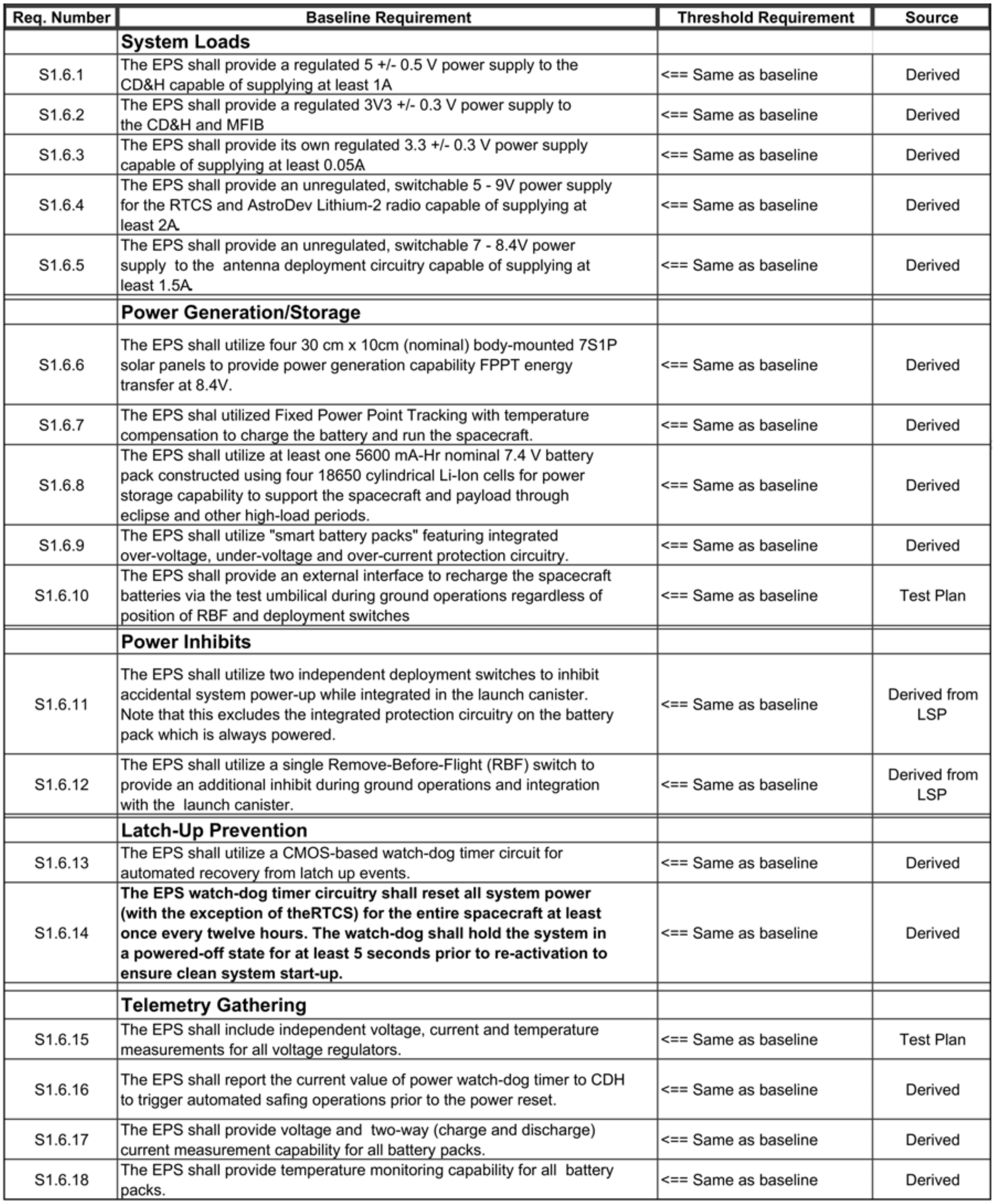
APPENDIX B

REQUIRMENT TABLES



Req. Number	Baseline Requirement	Threshold Requirement	Source
S1	**Flight System Requirements**		
	Payload accommodation		
S1-1	gRadSat shall accommodate the Computer Stack payload.	<== Same as baseline	M-1
S1-2	gRadSat shall provide a latching relay for raw uninterrupted power that has an independent battery protection. The relay shall be controlled by the avionics in the event of external failure detection.	<== Same as baseline	M-2 M-3
	Payload pointing		M-1
S1-4	gRadSat shall implement passive attitude control using a permanent magnet and hysteresis rods to dampen precession rates.	<== Same as baseline	M-1
	Payload data handling		
S1-5	gRadSat shall be capable of collecting and storing all Computer Stack data.	<== Same as baseline	M-4
	Spacecraft Systems		
S1-7	gRadSat shall utilize the SSEL FIREBIRD spacecraft bus, flight software and ground station architecture to the greatest extent possible.	<== Same as baseline	M-2 M-3 M-4

Figure B.1: Flight Systems Requirements



Req. Number	Baseline Requirement	Threshold Requirement	Source
	System Loads		
S1.6.1	The EPS shall provide a regulated 5 +/- 0.5 V power supply to the CD&H capable of supplying at least 1A	<== Same as baseline	Derived
S1.6.2	The EPS shall provide a regulated 3V3 +/- 0.3 V power supply to the CD&H and MFIB	<== Same as baseline	Derived
S1.6.3	The EPS shall provide its own regulated 3.3 +/- 0.3 V power supply capable of supplying at least 0.05A	<== Same as baseline	Derived
S1.6.4	The EPS shall provide an unregulated, switchable 5 - 9V power supply for the RTCS and AstroDev Lithium-2 radio capable of supplying at least 2A.	<== Same as baseline	Derived
S1.6.5	The EPS shall provide an unregulated, switchable 7 - 8.4V power supply to the antenna deployment circuitry capable of supplying at least 1.5A.	<== Same as baseline	Derived
	Power Generation/Storage		
S1.6.6	The EPS shall utilize four 30 cm x 10cm (nominal) body-mounted 7S1P solar panels to provide power generation capability FPPT energy transfer at 8.4V.	<== Same as baseline	Derived
S1.6.7	The EPS shal utilized Fixed Power Point Tracking with temperature compensation to charge the battery and run the spacecraft.	<== Same as baseline	Derived
S1.6.8	The EPS shall utilize at least one 5600 mA-Hr nominal 7.4 V battery pack constructed using four 18650 cylindrical Li-Ion cells for power storage capability to support the spacecraft and payload through eclipse and other high-load periods.	<== Same as baseline	Derived
S1.6.9	The EPS shall utilize "smart battery packs" featuring integrated over-voltage, under-voltage and over-current protection circuitry.	<== Same as baseline	Derived
S1.6.10	The EPS shall provide an external interface to recharge the spacecraft batteries via the test umbilical during ground operations regardless of position of RBF and deployment switches	<== Same as baseline	Test Plan
	Power Inhibits		
S1.6.11	The EPS shall utilize two independent deployment switches to inhibit accidental system power-up while integrated in the launch canister. Note that this excludes the integrated protection circuitry on the battery pack which is always powered.	<== Same as baseline	Derived from LSP
S1.6.12	The EPS shall utilize a single Remove-Before-Flight (RBF) switch to provide an additional inhibit during ground operations and integration with the launch canister.	<== Same as baseline	Derived from LSP
	Latch-Up Prevention		
S1.6.13	The EPS shall utilize a CMOS-based watch-dog timer circuit for automated recovery from latch up events.	<== Same as baseline	Derived
S1.6.14	**The EPS watch-dog timer circuitry shall reset all system power (with the exception of theRTCS) for the entire spacecraft at least once every twelve hours. The watch-dog shall hold the system in a powered-off state for at least 5 seconds prior to re-activation to ensure clean system start-up.**	<== Same as baseline	Derived
	Telemetry Gathering		
S1.6.15	The EPS shall include independent voltage, current and temperature measurements for all voltage regulators.	<== Same as baseline	Test Plan
S1.6.16	The EPS shall report the current value of power watch-dog timer to CDH to trigger automated safing operations prior to the power reset.	<== Same as baseline	Derived
S1.6.17	The EPS shall provide voltage and two-way (charge and discharge) current measurement capability for all battery packs.	<== Same as baseline	Derived
S1.6.18	The EPS shall provide temperature monitoring capability for all battery packs.	<== Same as baseline	Derived

Figure B.2: EPS Requirements

APPENDIX C

CODE

Resistor Selection Matlab Code

```
function B = GetRVal

vmp = 16.45;
TC = -6.7;
Vinreg = 2.7;
r = [1,1.02,1.05,1.07,1.1,1.13,1.15,1.18,1.2,1.21,1.24,1.27,1.3,...
    1.33,1.37,1.4,1.43,1.47,1.5,1.54,1.58,1.6,1.62,1.65,1.69,1.7,...
    1.74,1.78,1.8,1.82,1.87,1.91,1.96,2,2.05,2.1,2.15,2.2,2.21,...
    2.26,2.32,2.37,2.4,2.43,2.49,2.55,2.61,2.67,2.7,2.74,2.8,...
    2.87,2.94,3,3.01,3.09,3.1,3.16,3.22,3.24,3.33,3.32,3.4,3.48,...
    3.57,3.6,3.65,3.74,0.83,3.9,3.92,4.02,4.12,4.22,4.3,4.32,...
    4.53,4.64,4.7,4.74,4.75,4.87,4.99,5.05,5.1,5.11,5.23,5.36,...
    5.49,5.6,5.62,5.76,5.9,6,6.04,6.19,6.2,6.34,6.49,6.65,6.8,...
    6.81,6.98,7.15,7.25,7.32,7.5,7.68,7.87,8.06,8.2,8.25,8.45,...
    8.66,8.87,8.98,9.09,9.1,9.31,9.53,9.76,10,10,10.2,10.5,10.7,...
    11,11.3,11.5,11.8,12,12.1,12.4,12.7,13,13.3,13.7,14,14.3,...
    14.7,15,15.4,15.8,16,16.2,16.5,16.9,17,17.4,17.8,18,18.2,...
    18.7,19.1,19.6,20,20.5,21,21.5,22,22.1,22.6,23.2,23.7,24,...
    24.3,24.9,25.5,26.1,26.7,27,27.4,28,28.7,29.4,30,30.1,30.9,...
    31,31.6,32.2,32.4,33.3,33.2,34,34.8,35.7,36,36.5,37.4,8.3,39,...
    39.2,40.2,41.2,42.2,43,43.2,45.3,46.4,47,47.4,47.5,48.7,49.9,...
    50.5,51,51.1,52.3,53.6,54.9,56,56.2,57.6,59,60,60.4,61.9,62,...
    63.4,64.9,66.5,68,68.1,69.8,71.5,72.5,73.2,75,76.8,78.7,80.6,...
    82,82.5,84.5,86.6,88.7,89.8,90.9,91,93.1,95.3,97.6,100,100,102,...
    105,107,110,113,115,118,120,121,124,127,130,133,137,140,143,...
    147,150,154,158,160,162,165,169,170,174,178,180,182,187,191,...
    196,200,205,210,215,220,221,226,232,237,240,243,249,255,261,...
    267,270,274,280,287,294,300,301,309,310,316,322,324,333,332,...
    340,348,357,360,365,374,83,390,392,402,412,422,430,432,453,...
    464,470,474,475,487,499,505,510,511,523,536,549,560,562,576,...
    590,600,604,619,620,634,649,665,680,681,698,715,725,732,750,...
    768,787,806,820,825,845,866,887,898,909,910,931,953,976,1000,...
    1020,1050,1070,1100,1130,1150,1180,1200,1210,1240,1270,1300,...
    1330,1370,1400,1430,1470,1500,1540,1580,1600,1620,1650,1690,...
    1700,1740,1780,1800,1820,1870,1910,1960,2000,2050,2100,2150,
    2200,2210,2260,2320,2370,2400,2430,2490,2550,2610,2670,2700,...
    2740,2800,2870,2940,3000,3010,3090,3100,3160,3220,3240,3330,...
    3320,3400,3480,3570,3600,3650,3740,830,3900,3920,4020,4120,...
    4220,4300,4320,4530,4640,4700,4740,4750,4870,4990,5050,5100,...
    5110,5230,5360,5490,5600,5620,5760,5900,6000,6040,6190,6200,...
    6340,6490,6650,6800,6810,6980,7150,7250,7320,7500,7680,7870,...
    8060,8200,8250,8450,8660,8870,8980,9090,9100,9310,9530,9760,...
    10000];

%only the order of maginitude for the ratios matter.
%test = Resistors(vmp,Rset,TC,Vinreg,r);

for n=1:length(r);
  srset = r(n);
  all = Resistors(vmp,srset,TC,Vinreg,r);
  arrayvmp(n) = all(1);
  araryRset(n) = all(2);
  arrayRin1(n) = all(3);
  arrayRin2(n) = all(4);
 end


  tmp = abs(vmp-arrayvmp);
  [idx idx] = min(tmp) %index of closest value
  index =idx
  closest = arrayvmp(idx) %closest value
  araryRset(index)
  arrayRin1(index)
  arrayRin2(index)
```

```
function a = Resistors(vmp,Rset,TC,Vinreg,r)

Rin1 = -Rset*(TC/1000*4405);
Rin1 = close(Rin1,r);
Rin2 = Rin1/(((vmp+Rin1*(0.0674/Rset))/Vinreg)-1);
Rin2 = close(Rin2,r);

cvmp = ((Rin1*Vinreg)/Rin2-(337*Rin1)/(5000*Rset))+Vinreg;

a = [cvmp,Rset,Rin1,Rin2];
```

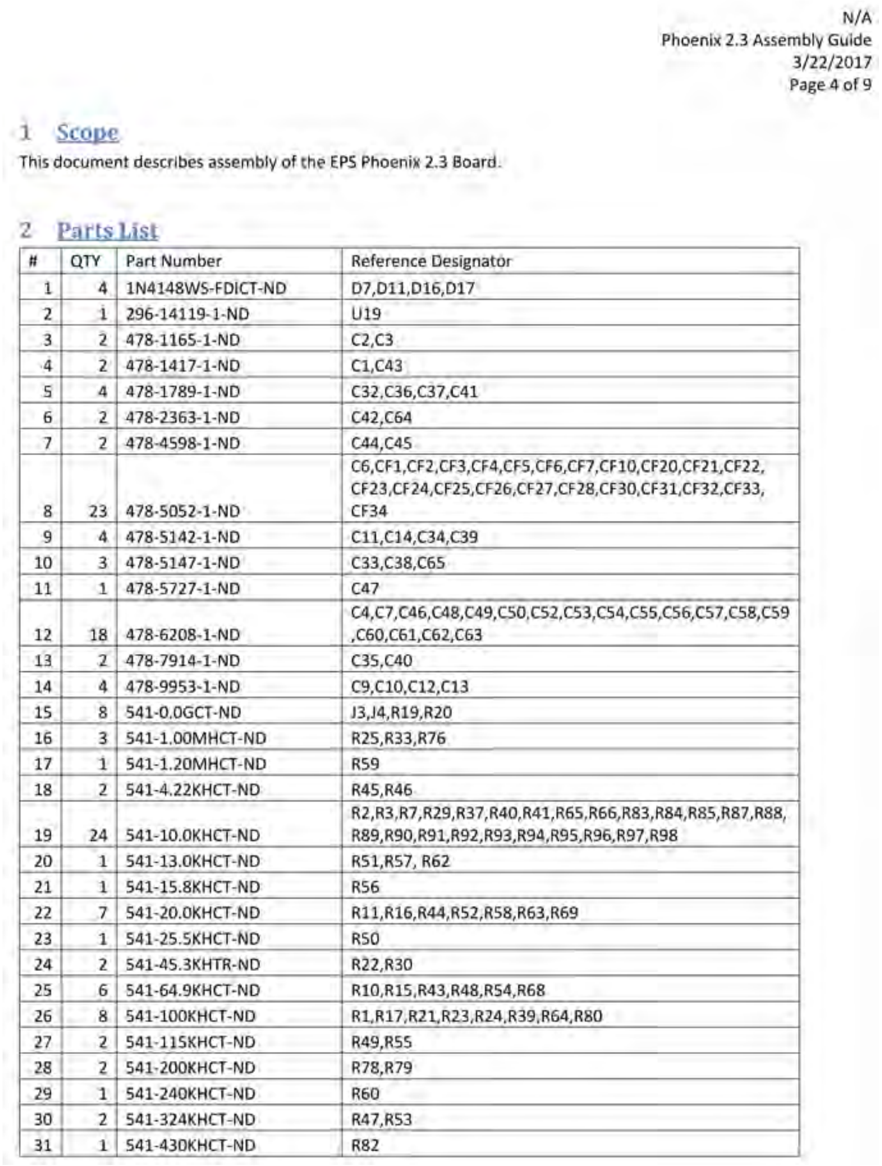
```
function A = close(val,r)

  tmp = abs(r-val);
  [idx idx] = min(tmp); %index of closest value
  closest = r(idx); %closest value
   A = closest;
```

APPENDIX D

DOCUMENT EXAMPLES

Fabrication Document Examples



N/A
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1 Scope

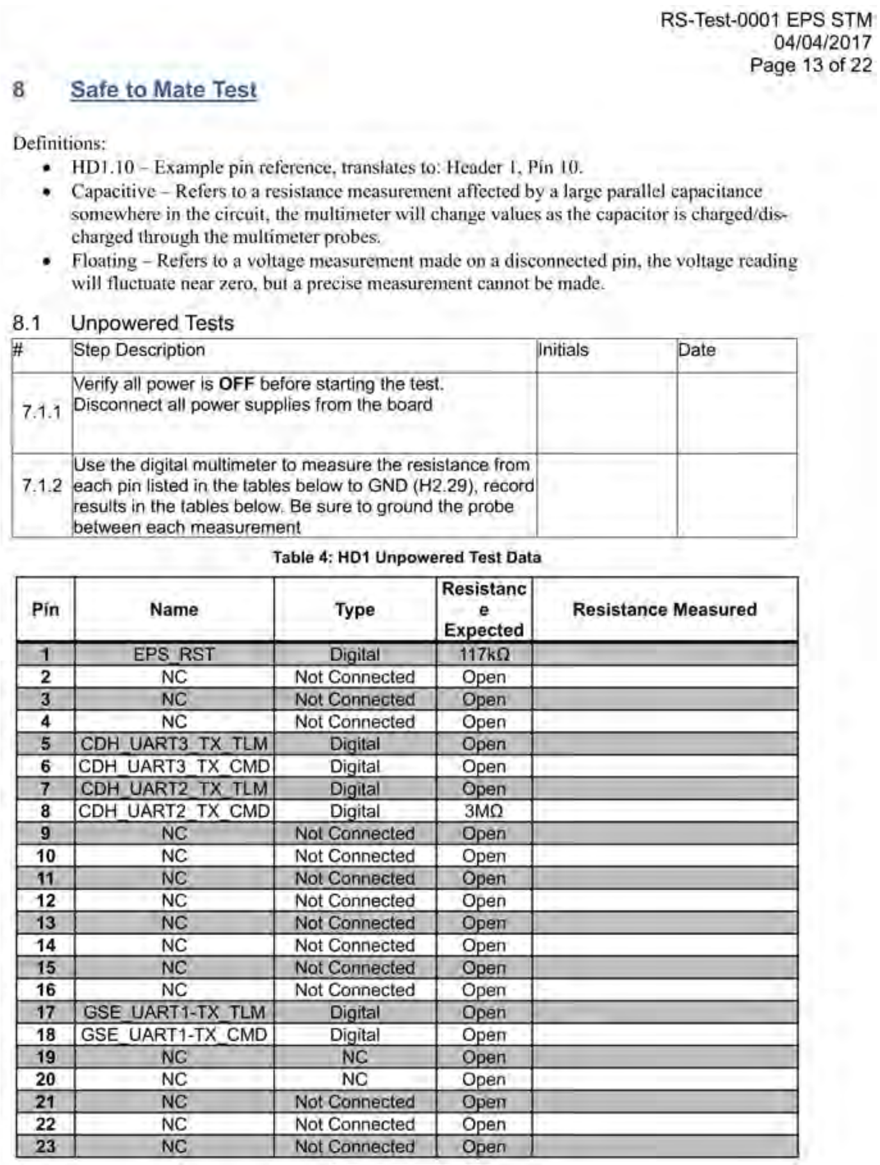
This document describes assembly of the EPS Phoenix 2.3 Board.

2 Parts List

#	QTY	Part Number	Reference Designator
1	4	1N4148WS-FDICT-ND	D7,D11,D16,D17
2	1	296-14119-1-ND	U19
3	2	478-1165-1-ND	C2,C3
4	2	478-1417-1-ND	C1,C43
5	4	478-1789-1-ND	C32,C36,C37,C41
6	2	478-2363-1-ND	C42,C64
7	2	478-4598-1-ND	C44,C45
8	23	478-5052-1-ND	C6,CF1,CF2,CF3,CF4,CF5,CF6,CF7,CF10,CF20,CF21,CF22, CF23,CF24,CF25,CF26,CF27,CF28,CF30,CF31,CF32,CF33, CF34
9	4	478-5142-1-ND	C11,C14,C34,C39
10	3	478-5147-1-ND	C33,C38,C65
11	1	478-5727-1-ND	C47
12	18	478-6208-1-ND	C4,C7,C46,C48,C49,C50,C52,C53,C54,C55,C56,C57,C58,C59 ,C60,C61,C62,C63
13	2	478-7914-1-ND	C35,C40
14	4	478-9953-1-ND	C9,C10,C12,C13
15	8	541-0.0GCT-ND	J3,J4,R19,R20
16	3	541-1.00MHCT-ND	R25,R33,R76
17	1	541-1.20MHCT-ND	R59
18	2	541-4.22KHCT-ND	R45,R46
19	24	541-10.0KHCT-ND	R2,R3,R7,R29,R37,R40,R41,R65,R66,R83,R84,R85,R87,R88, R89,R90,R91,R92,R93,R94,R95,R96,R97,R98
20	1	541-13.0KHCT-ND	R51,R57, R62
21	1	541-15.8KHCT-ND	R56
22	7	541-20.0KHCT-ND	R11,R16,R44,R52,R58,R63,R69
23	1	541-25.5KHCT-ND	R50
24	2	541-45.3KHTR-ND	R22,R30
25	6	541-64.9KHCT-ND	R10,R15,R43,R48,R54,R68
26	8	541-100KHCT-ND	R1,R17,R21,R23,R24,R39,R64,R80
27	2	541-115KHCT-ND	R49,R55
28	2	541-200KHCT-ND	R78,R79
29	1	541-240KHCT-ND	R60
30	2	541-324KHCT-ND	R47,R53
31	1	541-430KHCT-ND	R82

Figure D.1: Excerpt of Assembly Guide

Analysis Document Examples



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8 Safe to Mate Test

Definitions:

- HD1.10 – Example pin reference, translates to: Header 1, Pin 10.
- Capacitive – Refers to a resistance measurement affected by a large parallel capacitance somewhere in the circuit, the multimeter will change values as the capacitor is charged/discharged through the multimeter probes.
- Floating – Refers to a voltage measurement made on a disconnected pin, the voltage reading will fluctuate near zero, but a precise measurement cannot be made.

8.1 Unpowered Tests

#	Step Description	Initials	Date
7.1.1	Verify all power is **OFF** before starting the test. Disconnect all power supplies from the board		
7.1.2	Use the digital multimeter to measure the resistance from each pin listed in the tables below to GND (H2.29), record results in the tables below. Be sure to ground the probe between each measurement		

Table 4: HD1 Unpowered Test Data

Pin	Name	Type	Resistance Expected	Resistance Measured
1	EPS_RST	Digital	117kΩ	
2	NC	Not Connected	Open	
3	NC	Not Connected	Open	
4	NC	Not Connected	Open	
5	CDH_UART3_TX_TLM	Digital	Open	
6	CDH_UART3_TX_CMD	Digital	Open	
7	CDH_UART2_TX_TLM	Digital	Open	
8	CDH_UART2_TX_CMD	Digital	3MΩ	
9	NC	Not Connected	Open	
10	NC	Not Connected	Open	
11	NC	Not Connected	Open	
12	NC	Not Connected	Open	
13	NC	Not Connected	Open	
14	NC	Not Connected	Open	
15	NC	Not Connected	Open	
16	NC	Not Connected	Open	
17	GSE_UART1-TX_TLM	Digital	Open	
18	GSE_UART1-TX_CMD	Digital	Open	
19	NC	NC	Open	
20	NC	NC	Open	
21	NC	Not Connected	Open	
22	NC	Not Connected	Open	
23	NC	Not Connected	Open	

Figure D.2: Excerpt of Safe To Mate Document