A Survey of Radiation Hardened CMOS Techniques

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I) Introduction:

The universe we live in is surrounded and filled with vast amounts of radiation[14]. As we indulge more and more into exploring our universe it becomes necessary to come up with technology that can tolerate if not combat the radiation in space. Over the past few decades a number of robotic and manned space exploration systems have been realized throughout the world. Satellites and space shuttles containing thousands of electronic circuits get flown into space to read and record the observed data. Clearly these electronic devices would not be of much use if they were intolerant to radiation in space and malfunctioned regularly. For this reason, radiation, its effects on the electronics and different methods to prevent or correct the adverse effects of radiation on electronics circuits have become a large area of research in aerospace engineering. The designing and realizing of circuits or devices which are tolerant to radiation is called as the "radiation hardening" of the circuit or device. Meaning to say that these devices or circuits are "hardened" to the effects of radiation and hence the name "Rad-hard devices".

Of the many technologies that are used for the implementation of these devices like CMOS, BJT and FPGA technologies to name a few, CMOS circuits have gained huge popularity as a favorable option for space electronics because of the advantages they posses like small size, high speed and most importantly their low power consumption capability as low power consumption is the primary consideration for devices in space [1].

II) Sources of space radiation

Radiation can be defined as energy in transit in the form of high-speed particles and electromagnetic waves [16]. "Space radiation", is the term that is used to refer to the radiation that exists around and beyond our planet [16]. Even though non-ionizing radiation like radio waves, and visible light exist, ionizing radiation is what forms the larger part of space radiation [14, 16]. Ionizing radiation possesses very high energy and hence the ability to displace electrons from their orbits when it comes in contact with atoms [14]. This causes the atoms to become highly reactive particles called "ions" which explains why this particular radiation is called "ionizing" radiation. As non-ionizing radiation does not contain enough energy to disturb the atomic structure of particles, radiation hardening techniques are primarily focused on combating the effects of ionizing radiation [14].

The three main sources of ionizing radiation in space are [16]

a) Galactic cosmic radiation
b) Solar particle events and
c) Trapped radiation

Each of these types of radiation is discussed below in detail.

A. *Galactic cosmic radiation.*

This radiation is caused by high speed and low flux cosmic rays which originate outside the solar system. They comprise 85% protons, 14% alpha particles and 1% heavier nuclei like iron, cobalt and nickel. Satellites and spacecrafts are protected to an extent from the galactic cosmic radiation as the earth's magnetic field provides a good shield against them. However the geo-magnetic shield is almost non-existent near the Polar Regions where the earth's magnetic lines are not as strong [16].

B. *Solar particle events.*

Solar flares and Coronal mass ejections cause solar particle events which are bursts of energetic particles and electromagnetic rays that are injected into inter-planetary space. They mostly comprise of protons with electrons and alpha particles in small quantities. The earth's geomagnetic field provides a good shielding to space electronics from the solar protons, for the most part of the sun's 11-year cycle (7 active years called the solar maximum and 4 inactive years called the solar minimum). However the sun has one or two very large bursts during its solar maximum period which can cause permanent damages to electronic circuits and devices in space crafts [16].

C. *Trapped radiation.*

The sun produces a constant stream of particles called the solar wind which mainly consist of electrons and protons and a small percentage of ions. The earth's magnetic field forms a "magnetosphere" around itself which deflects most of these particles. However some of these particles do not get deflected by the earth's magnetosphere and get trapped in one of the two magnetic rings around the planet. These magnetic rings or belts have high radiation energy and are called the Van-Allen radiation belts. The inner belt mostly consists of a stable population of protons with energies exceeding 10 MeV and the outer belt contains mainly electrons with energies up to 10 MeV [16].

III) Effects of radiation on CMOS electronics

The two primary effects that radiation has on CMOS electronics is [3]

a) Effects due to total ionizing dose and
b) Single event effects

A Total Ionizing Dose (TID)

When materials are subjected to ionizing radiation, the electrons in valence bands get enough excitation to enter the conduction bands. This ionization process causes energy to be trapped in the materials and is called “dose” or “total ionizing dose (TID)”. The unit of measurement for TID is “rads” or “Grays”. The two main problems caused by total ionization dose in CMOS circuits are discussed below [14].

A1 Oxide Doping

When an ionizing particle or radiation passes through a MOS structure, electron hole pairs are generated in the particles path. As the resistance in the substrate and the gate is low, the electron-hole pairs quickly disappear. In the oxide however, only a small fraction of the electron-hole pairs recombine while the rest of the electron-hole pairs stay trapped in the oxide. Silicon dioxide is an insulator and electrons and holes have different mobilities in the oxide. They differ by a six to twelve orders of magnitude. In such a case when a positive bias is applied to the gate, the electrons move towards the gate faster than the mobility of holes (which move towards the substrate). This causes the holes to be “trapped” in the oxide causing the oxide to have a fixed positive charge [1].

As the oxide layer acts as the barrier between the metal and the semiconductor layers in a MOS device, the trapped positive charge can

a) Lower the barrier temporarily

b) Capture the charge that is passing through the oxide and form a semi-permanent charge sheet.

c) Alter the gate-to-channel potential in MOS devices, causing threshold voltage shifts.

d) Disturb the liable bonds that occur at the semi-conductor/oxide interface [1].

A2 Substrate Leakage Current

Substrate leakage current occurs when a current path is formed in the substrate/oxide interface. This leakage current affects the functioning of the device as the device stays turned “on” even with no gate voltage [3, 5].

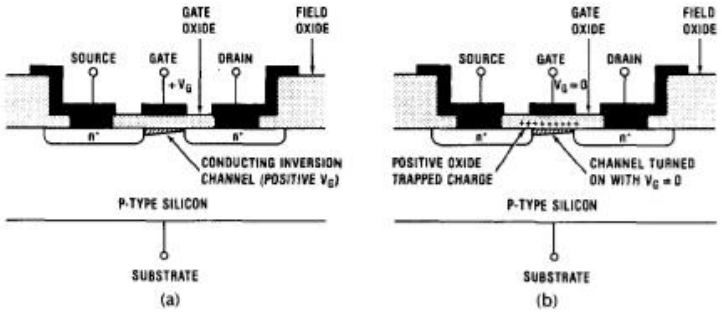

Figure 1: (a) Normal functioning of a transistor. (b) Transistor turned on even without any gate voltage [3].

B Single Event Effects

B1 Single Event Transients

When a heavy ion hits an electronic device and passes through a sensitive node, it generates a transient voltage pulse at that node. This is called a single event transient [14].

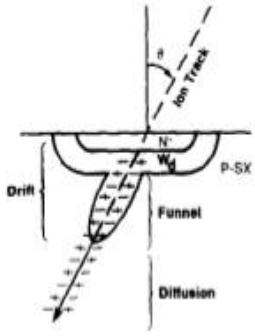

Figure 2: The ionizing path when an ion hits the diffusion region [1].

B2 Single Event Upsets

When the heavy ion hits a sensitive node such as a diffusion region in a MOS device the subsequent SET induces ionization in that area which often causes a change in the logical state. These errors in states are termed as “single event upsets” [1, 14].

B3 Single-Event Latch-up

The ionization pulse induced by the heavy ions can cause the p-n-p-n thyristor structure (that is present in bulk CMOS circuits) to turn on. This causes a low-impedance structure to be maintained between the cathode and the anode and the thyristor remains on for the entire low-impedance period. This is called a latch up and is a very destructive effect caused by ionizing radiation as it causes the device to not respond to any control signals [1, 3]

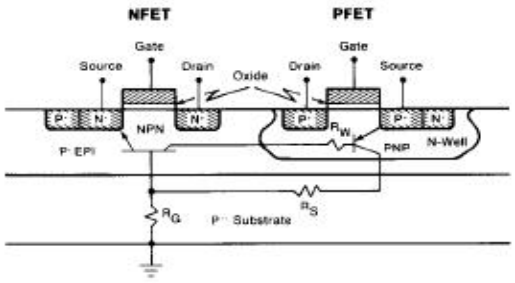

Figure 3: The parasitic p-n-p-n thyristor [1].

IV) Existing Solutions

A. Materials/Process

C1 Substrate doping

Substrate doping reduces the charge collection at the substrate-oxide interface. High doping concentrations at the interface hinder the progress of an ion track as lesser number of electron-hole pairs are formed when exposed to ionizing radiation. It also prevents the formation of the channel that is the substrate leakage current when the transistor is not biased [1].

C2 Thin oxide

The holes that get trapped in the oxide cause threshold voltage shifts and threaten the proper functioning of the circuit. By reducing the thickness of the oxide the number of holes that can be formed in it is also reduced. Thus thin oxide devices tend to be more radiation hardened than devices with a thick oxide [1].

B. Physical layout techniques

C1 Enclosed layout transistors and guard rings

Enclosed layout transistors are very effective in preventing the substrate leakage currents. The drain or the source is enclosed within the gate region and the other diffusion region surrounds the gate region. This eliminates the parasitic path connecting the drain and source through the substrate. Guard rings are also used to prevent leakage current. The n channel transistors are enclosed by a p+ guard ring and the p-channel transistor is enclosed by an n+ guard ring. The p+ guard rings decrease the gain of the NPN parasitic bipolar transistor, introducing a strongly doped p region in the base and keeping the base firmly close to ground. The n+ guard rings acts in a similar way with the PNP parasitic bipolar transistor [10, 11].

C2 Large critical charge Q_{crit} .

The critical charge level "Q_{crit}" is the minimum charge that needs to be collected at the sensitive node to cause an upset. When a single event hit occurs it results in an excess of minority charge carriers at the depletion region. These charge carriers collect at the sensitive node, and cause a single event transient to be produced. This results in a bit-flip or loss of information. The critical charge level can be increased by increasing the capacitance of the devices. This however is not one of the best radiation hardening

techniques as increasing the capacitance requires the devices to be larger and the circuit speed is reduced [1].

C. *Circuit Level Solutions*

C1 Clamping diodes

This approach uses a clamping circuit to protect the output of the gate in case of irradiation. When radiation strikes a diffusion node, it causes voltage glitches at the node. The clamping circuit is arranged such that this glitch gets clamed before it reaches the switching point so that the devices do not change their logic state [2].

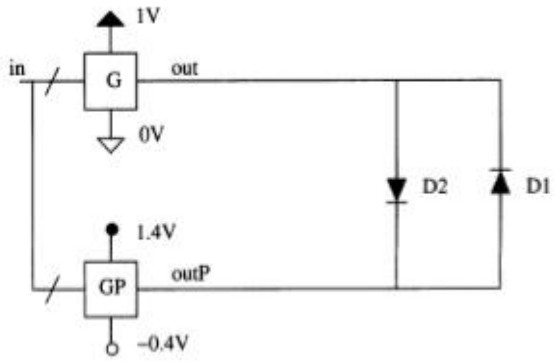

Figure 4: The clamping circuit [2].

The figure shows the clamping circuit formed by the diodes, connected to two devices. Logic gate ‘G’ is the gate that needs to be protected and the logic gate ‘GP’ is an identical gate that is connected to the circuit so as to not let the clamping diode circuit interfere with the normal functional operation of the gate [2].

C2 Shielding

Shielding is used to protect the integrated circuits from bombardment by large particles. The packaging of the IC is done with polyimide layers which shield the circuits within from alpha particles and the resulting decay products. Shielding does not protect the devices from single event upsets [1, 3].

D. Logical Solutions

D1 Triple modular redundancy (TMR)

TMR is a fault tolerant technique implemented in integrated circuits. In this scheme there exist three identical circuits or systems which performing the same task for

the same data. At the end of the cycle all the three outputs are gathered and compared by a fourth "monitoring" device or circuit. If at least two of the three devices result in the same output, that output is considered to be the output of the system. In the TMR scheme the result is processed by a voting system to produce a single output. If any one of the three systems fails, the other two systems can mask the fault [8, 9].

D2 Temporal Redundancy

Temporal redundancy is a scheme where a circuit separates identical data signal in time in order to filter out single event upsets. It is similar to the TMR scheme, only TMR is a spatial redundancy technique which separates identical data in space and the TR scheme separates identical data in time [17].

V) Conclusion and future work:

A review of the effects of radiation on CMOS circuits and some of the existing solutions is presented in the paper. All of the radiation hardened techniques discussed in this paper have tradeoffs between hardness, performance and cost. Clearly future work is needed to investigate cost-effective rad-hard techniques which do not greatly affect the performance of the circuits.

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