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Off-Chip Coaxial-to-Coplanar Transition Using MEMs Trench

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***Abstract*- This paper presents the electromagnetic Finite Element Analysis (FEA) of a novel chip-to-chip interconnect for use in System-in-Package (SiP) applications. An on-chip coplanar transmission line is transitioned to an off-chip coaxial cable using an etched trench on Silicon. This approach to die-to-die signaling has inherent advantages over traditional wire bonding that include matched impedance, shielded signal conductors, and low impedance return paths. This paper presents the analysis of the impedance discontinuities associated with the transition between the two controlled impedance structures (coplanar and coaxial) in order to understand if the manufacturing processes used affects the ideal operation of this structure. We show that this type of die-to-die interconnect system reduces the parasitic inductance of the signal path by 57% and that reflections are reduced by 75% compared to a traditional wire bond.**

I. Introduction

Off-chip SSN is a critical problem in System-in-Package (SiP) applications. One such application is the interface between a microprocessor and memory configured as two independent chips on a single package substrate. This type of configuration decreases the physical size of the total interconnect because the connection is only made to the package. This approach has the advantage of using smaller interconnect, which has less parasitic inductance and capacitance. It also attempts to exploit the cost advantages of design segmentation. This type of system is still limited by the overall interconnect because the same mechanical connections are used as in the chip-to-board connection, albeit at a smaller scale.

Another SiP application that suffers from off-chip interconnect deficiencies is the integration of CMOS processing and wireless communication. SiP has the inherent advantage that different circuit substrates can be used in a single package. This allows the optimal material to be chosen for the application. Silicon has long been the material of choice for digital CMOS circuitry due to its low static power consumption. However, when interfacing to a wireless signal, Silicon Germanium (SiGe) tends to be a better material for telecommunications circuits such as amplifiers and mixers which require more power. SiP allows application specific materials to be used and interfaced using package interconnect. In this situation, a high quality interconnect is of great importance on the package because the signals are often high frequency and analog in nature. Getting a high quality analog connection between SiGe and Silicon can enable Silicon-based Analog-to-Digital Conversions (ADC) and demodulation via Digital Signal Processing (DSP). These functionally diverse systems have great promise but will ultimately be limited by the lack of a high speed connection between multiple substrates within the same package.

We have performed an initial feasibility study on creating a micro-scale, coaxial-to-coplanar launch for use as an off-chip interconnect in SiP applications. A Silicon substrate which contains controlled impedance coplanar transmission lines is processed using a Micro Electrical Mechanical System (MEMS) fabrication sequence in order to create an anisotropic trench. A miniature coaxial cable with extended center conductor is placed into the trench such that the center conductor of the coax is coincident to the signal trace of the coplanar structure. The outer shield of the coaxial cable is coincidence to the outer ground traces of the coplanar structure, thus completing the electrical connection. This type of off-chip interconnect system provides shielding for the signal path in addition to a controlled and dedicated path for the return current. This will inherently reduce SSN and enable a higher speed connection between dies residing on the same package substrates. Figure 1 shows our proposed system.

In this paper, we present the computer analysis and simulations on the proposed interconnect system. Electromagnetic Design Systems (EMDS) software from *Agilent Technologies* is used to perform Finite Element Analysis (FEA) in order to predict the electrical performance of the system.

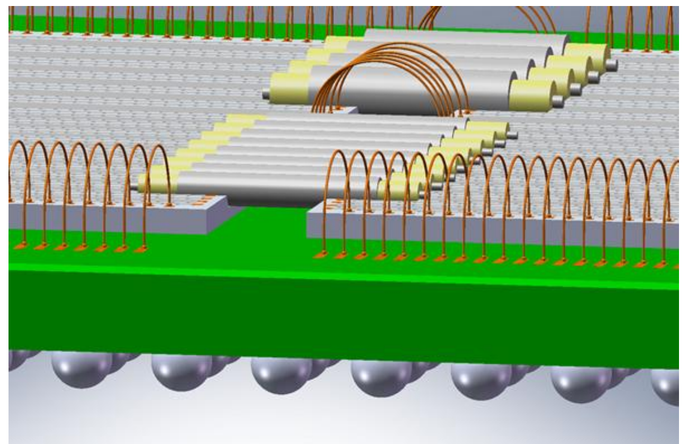

Figure 1. 3D Rendering of our proposed system showing miniature coaxial cables mounted to adjacent dies in an SiP application. Our approach is used in conjunction with traditional wire bonds.

II. Methodology

Micro-ElectroMechanical Systems (MEMS) fabrication technology has advanced in recent years to produce commercially viable products used in the automotive and biomedical fields. The ability to reliably form mechanical features on an IC substrate has created an opportunity to apply novel approaches to the off-chip interconnect problem. Using micro-scale CMOS processes to form MEMS features enables a new approach to increasing the throughput of SiP systems.

MEMS technology can be adapted to form an off-chip coaxial to coplanar launch for the transport of high-speed digital signals. In this approach, in order to form the new connection we add a coplanar transmission line, then a trench is etched into the IC substrate. The center conductor of the coaxial cable is laid onto an exposed outer layer of the signal trace of a coplanar interconnect. Both ground traces on the coplanar are connected to the coaxial outer shield in order to provide a return path for the signal. This approach yields a controlled impedance path to transmit signals on and off of the IC using shielded conductors. Figure 2 shows the top and side views of this approach.

This approach has inherent advantages. The first is that the shielding of the coaxial conductor eliminates any coupling within the package interconnect. The second is that size of the interconnect can be miniaturized relative to existing interconnect technologies. One of the reasons that modern interconnect is large relative to on-chip feature sizes is the mechanical assembly processes that are used. The machines that handle the interconnect have limited accuracy so the feature sizes must be large enough to overcome this error. The MEMS trench in this approach has inherent alignment features that reduce the error of robotic assembly. When the mini-coax is placed into the trench, a downward vertical force can be applied to the coax and the trench will automatically align the center conductor to the signal trace of the coplanar on the IC as the coax slides downward. With this alignment issue addressed, the physical size of the interconnect can be reduced which leads to increased electrical performance.

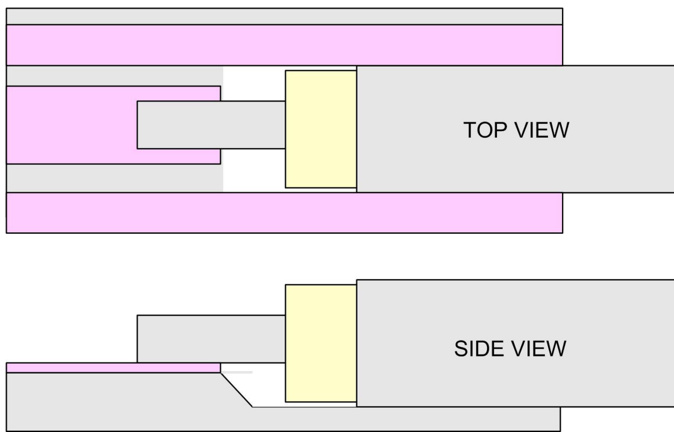

Figure 2. Top and side view of off-chip coaxial to coplanar launch using MEMS trench.

III. Finite Element Analysis

The design shown in figure 2 has 8 major cross-sections. The first step in examining the feasibility of this approach is to examine the spatial considerations of such a design. Then the electrical parameters can be compared between the new interconnect and existing off-chip interconnect to evaluate the improvements.

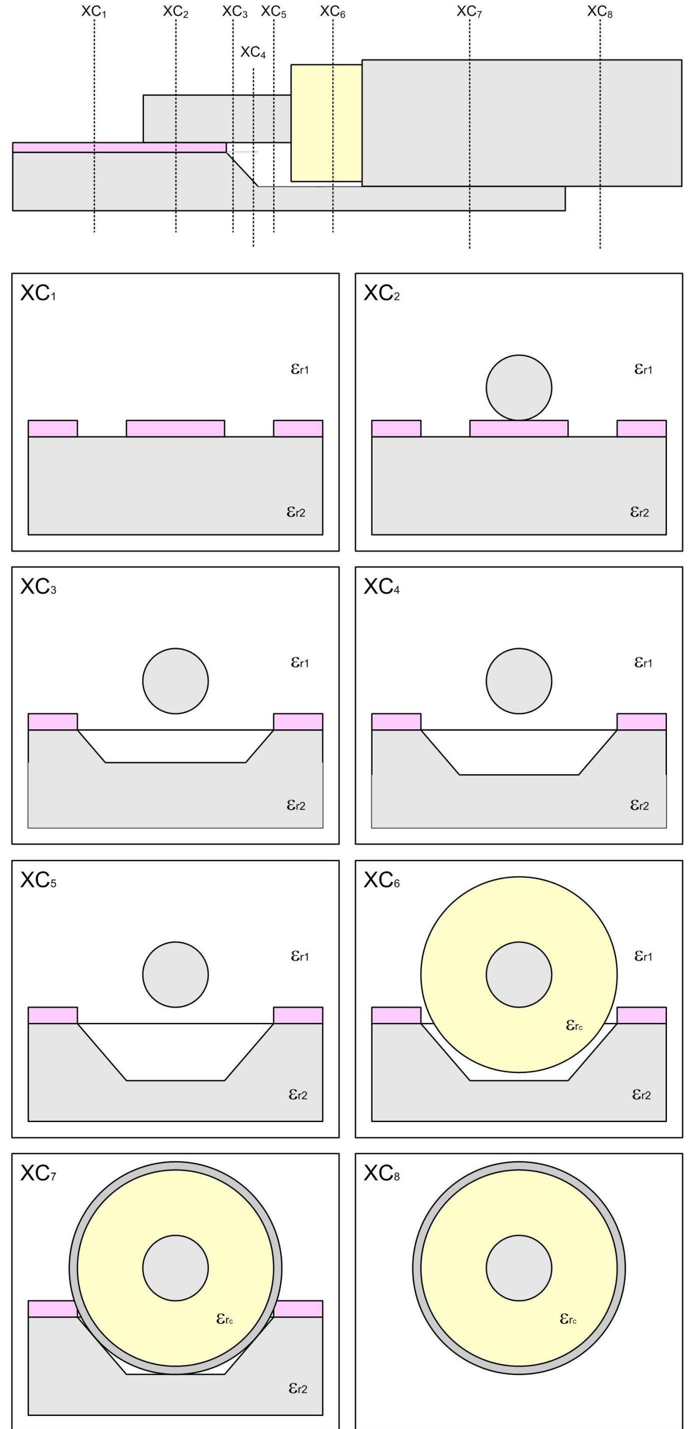

Figure 3. Cross sections of the coaxial to coplanar launch.

EMDS from *Agilent Technologies* was used to perform the 2D and 3D field solver FEA. 2D analysis for each of the cross sections defined in figure 3 was performed in order to extract the characteristic impedance (Z_O) and the propagation constant (g) as a first step to create a complete model for SPICE simulations. Figures 4-11 shows the field lines from the 2D solver.

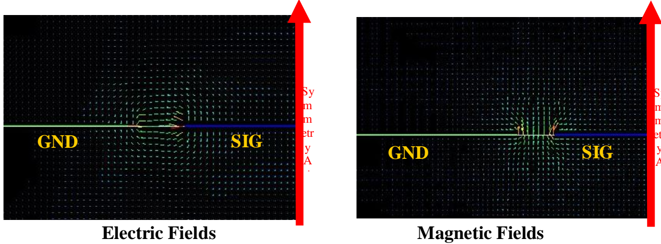

Figure 4. Cross section 1 electric and magnetic fields.

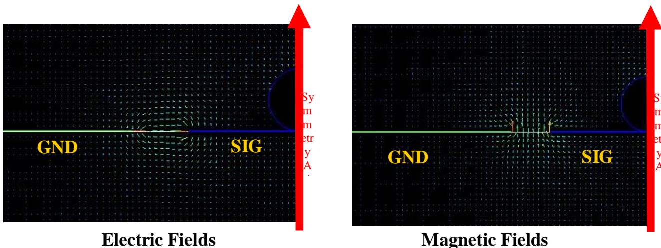

Figure 5. cross section 2 electric and magnetic fields.

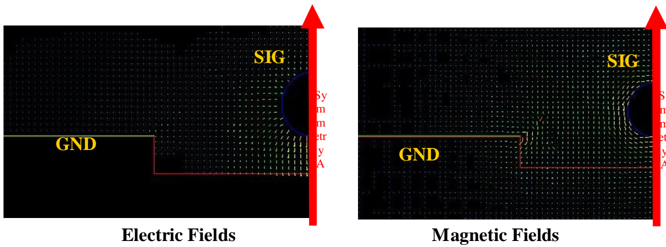

Figure 6. Cross section 3 electric and magnetic fields.

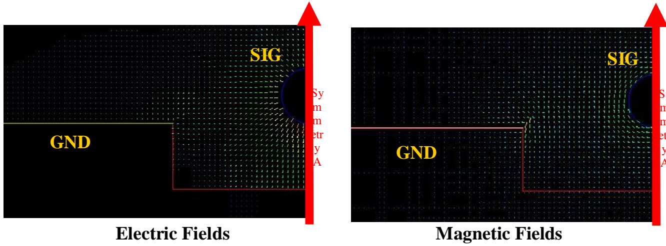

Figure 7. Cross section 4 electric and magnetic fields.

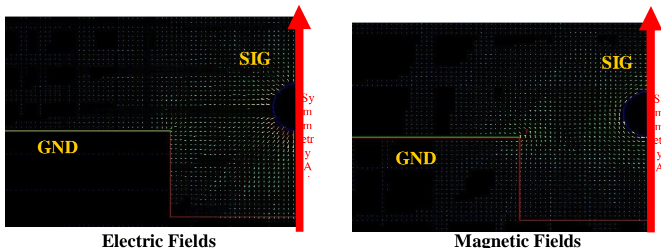

Figure 8. Cross section 5 electric and magnetic fields.

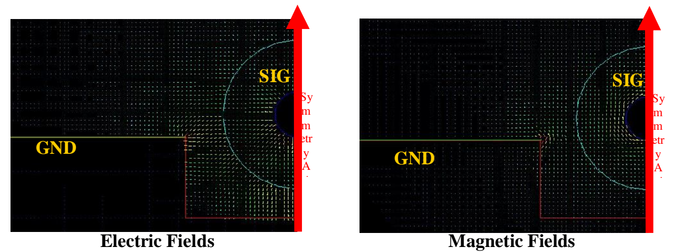

Figure 9. Cross section 6 electric and magnetic fields.

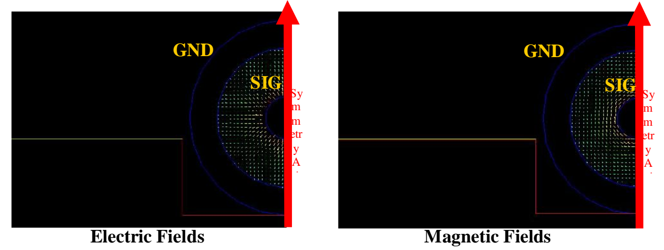

Figure 10. Cross section 7 electric and magnetic fields.

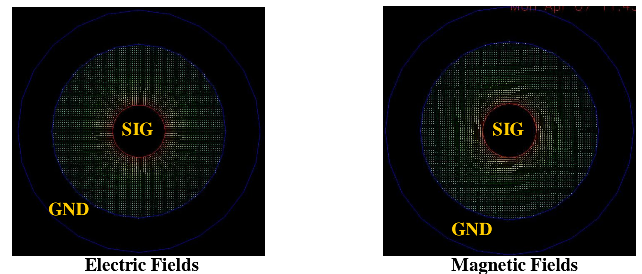

Figure 11. Cross section 8 electric and magnetic fields.

Table 1. shows the characteristic impedance and propagation constant for each cross section as determined from the 2D field solver:

Region	Z_O	g
XC1	52 + j26	305 + j615
XC2	50 + j25	299 + j604
XC3	114 + j3	10 + j269
XC4	128 + j1	4 + j239
XC5	134 + j1	3 + j229
XC6	111 + j1	5 + j276
XC7	50 + j0	0 + j296
XC8	50 + j0	0 + j296

Table 1. Characteristic Impedance and Propagation Constant for each cross-section of the interconnect transition.

In order to understand if the coaxial to coplanar launch can improve electrical performance, the parasitic capacitance and inductance are calculated and compared to standard package interconnect types. In the proposed launch, the majority of the interconnect length resides in the coaxial portion of the line. We will compare the coaxial portion of the interconnect to a traditional wire bond, which is the most common types of interconnect for connecting an multiple IC substrates.

For this case, the wire bond used is a 25 µm diameter, gold wire which forms a ball bond on the Silicon substrates using 100µm x 100µm pads [22]. Table 2 shows the parasitics of our approach versus a traditional wire bond for a 3mm length of die-to-die interconnect.

Parameter	Units	Wire Bond	Coaxial Line
L'	nH/m	569	242
C'	pF/m	26	97
Zo	Ω	148	50
L_{3mm}	nH	1.71	0.73
C_{3mm}	pF	0.08	0.29

Table 2. Electrical parasitics for the two types of die-to-die interconnect that were evaluated.

This table illustrates that by moving to the coaxial off-chip interconnect, the parasitic inductance can be reduced by 57% and the parasitic capacitance by 66% over a wire bond. In addition, the impedance of the coaxial line can be controlled to yield a standard 50Ω transmission line versus the uncontrolled 148Ω impedance of the wire bond.

A transient analysis was conducted on the new launch by simulating the Time Domain Reflectrometry (TDR) and Time Domain Transmission (TDT) responses. This type of analysis was performed by creating an equivalent SPICE model from the 2D field solver results in table 1. 12 shows the TDR and TDT result of the simulations.

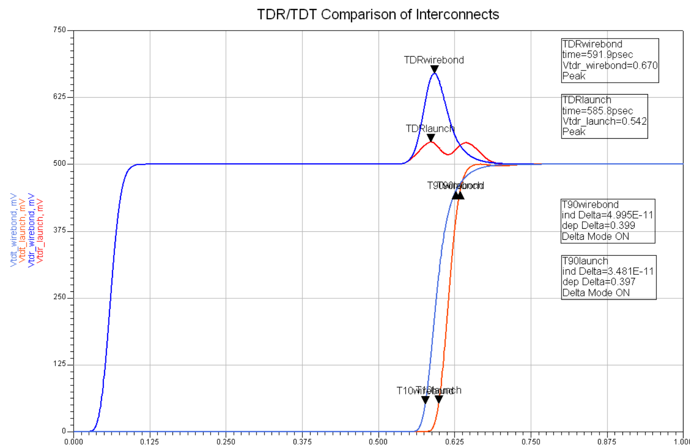

Figure 12. TDR/TDT simulation results for a 35ps input step.

This comparison showed that the coax launch reflections are equal to 8% of the original signal, while the wire bond reflections are equal to 34% of the original signal.

In order to complete our electrical analysis, we stimulated the system with a pseudo random bit sequence (2^4-1) and observed the eye diagram at a data rate of 5Gb/s using a source risetime of 35ps. Figure 13 and 14 show the eye diagrams of the wire bonded system and coplanar-to-coaxial system respectively.

These results illustrate that the coaxial-to-coplanar launch has significant electrical advantages over the standard off-chip interconnect technology currently being used and is worth further investigation.

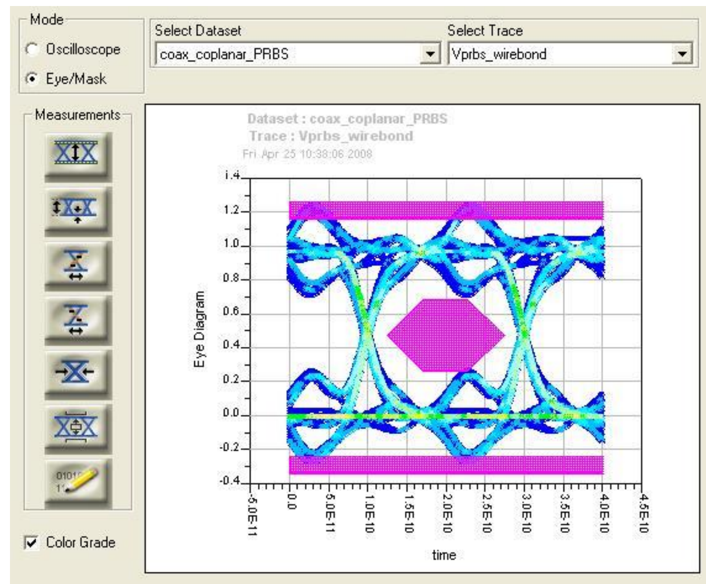

Figure 13. Eye Diagram for wire bond at 5Gb/s.

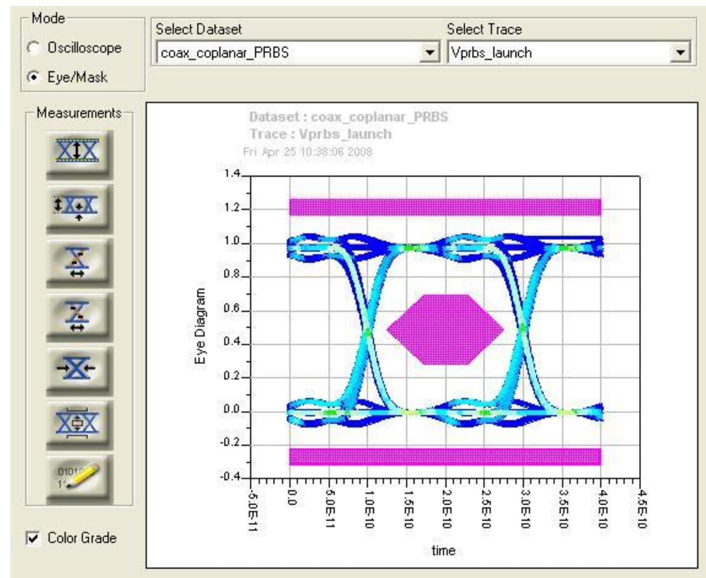

Figure 14. Eye diagram for the coaxial-to-coplanar interconnect at 5Gb/s

CONCLUSION

This paper presented the electrical simulation analysis of a novel die-to-die interconnect system that consists of a coaxial to coplanar transition using an etched trench. It was shown that the new interconnect structure reduced the parasitic inductance of the off-chip interconnect by 57% compared to the traditional wire bond for a length of 3mm. The new structure also reduced reflections due to the interconnect by 75% compared to a wire bond. The coaxial to coplanar interconnect system evaluated presents a novel solution to the electrical limitations of modern package interconnect.

REFERENCES

[1] M. Miura, N. Hirano, Y. Hiruta, and T. Sudo, "Electrical Characterization and modeling of simultaneous switching noise for leadframe packages", *Proceedings of the 45th Electronic Components and Technology Conference*, pp. 857-864, May 1995.

[2] M. Miura, N. Hirano, Y. Hiruta, and T. Sudo, "Characterization and Reduction of Simultaneous Switching Noise for a Multilayer Package", *Proceedings of the 44th Electronic Components and Technology Conference*, pp. 949-956, May 1994.

[3] B. Young, "Return path inductance in measurements of package inductance matrixes", *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, vol. 20, pp. 50-55, Feb 1997.

[4] "The International Technology Roadmap for Semiconductors", www.itrs.net, 2006.

[5] R. Campbell, M. Andrews, T. Lesher, & C. Wai, "220GHz Wafer Probe Membrane Tips and Waveguide-to-Coax Transitions", *2005 European Microwave Conference*, vol. 2, pp. 4-7, Oct 2005.

[6] A. Penirschke, J. Freese, J. Biebelt, B. Allenbert, & R. Jakoby, "Novel Integrated Coaxial Line to Cylindrical Waveguide Directive Couplers in Pipelines for Process Monitoring Applications", *2005 IEEE MTT-S International Microwave Symposium Digest*, pp 1203-1206, June 2005.

[7] M. Pardalopoulou, K. Solbach, "Over-moded Operation of Waveguide-to-Coax Transition at 60GHz", *12th International Conference on Terahertz Electronics*, pp. 475-476, Sept 2004.

[8] W. Kanghan, C. Zhihong, Z. Yumei, & H. Jinzhong, "A Novel Coaxial Probe Waveguide to Microstrip Transition", *Proceedings of the 2005 Asia-Pacific Microwave Conference (APMC)*, vol. 1, pp. 3, Dec 2005.

[9] G. Hopkins, B. Edenfield, J. Hampton, & R. Roberts, "A New Coax to Troughguide Transition", *IEEE Microwave and Wireless Components Letters*, vol. 12, issue 8, pp. 299-301, Aug 2002.

[10] R. Chen, E Brown, & R Singh, "A Compact 30GHz Low Loss Balanced Hybrid Coupler Fabricated Using Micromachined Integrated Coax", *2004 IEEE Radio and Wireless Conference*, pp. 227-230, Sept 2004.

[11] R. Chen, E Brown, & C. Bang, "A Compact Low Loss Ka-band Filter Using 3-Dimensional Micromachined Integrated Coax", *17th IEEE International Conference on Micro Electro Mechanical Systems*, pp. 801-804, Sept 2004.

[12] M. Morgan, S. Weinreb, "A Millimeter-Wave Perpendicular Coax-to-Microstrip Transition", *2002 IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 817-820, June 2002.

[13] S. Banerjee, R. Drayton, "Micromachined Low Dispersion Interconnects for Optoelectronic Array Packaging", *2005 IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp 1565-1568, June 2005.

[14] Y. Hao and D. Zhang, "Silicon-based MEMs process and standardization", *Proceedings of the 7th International Conference on Sold-State and Integrated circuits Technology*, vol. 3, pp. 1835-1838, 2004.

[15] A. Beliveau, G.T. Spencer, K.A. Thomas, and S.L. Roberson, "Evaluation of MEMS Capacitive Accelerometers", *IEEE Design and Test of Computers*, vol. 16, no. 4, pp. 48-56, Dec 1999.

[16] T.J. Kaiser, B.J. Lutzenberger, R.A. Friholm, P.A. Himmer, and D.L. Dickensheets, "Silicon Nitride Biaxial Pointing Mirrors with Stiffening Ribs", *Proceedings of the 2001 SPIE Conference on Micromachining and Microfabrication*, pp 278-282, 2001.

[17] B.J. Lutzenberger, D.L. Dickensheets, and T.J. Kaiser, "Large Area Molded Silicon Nitride Micro Mirrors", *IEEE Photonics Letters*, vol. 15, no. 10, pp. 1407-1409, 2003.

[18] W. Dally, and J. Poulton, "Digital Systems Engineering", *Cambridge University Press*, 2001.

[19] High Speed Cable Design Guide, Samtec Inc., www.samtec.com.

[20] Fine Wire Guide, Tyco Electronics Inc., www.precisioninterconnect.com.

[21] R. Tummala, "Fundamentals of Microsystems Packaging.", *McGraw-Hill*, 2001.

[22] B.J. LaMeres, S.P. Khatri "Broadband Impedance Matching for Inductive Interconnect in VLSI Packages", *IEEE International Conference on Computer Design (ICCD)*, Oct. 2005.