DesignCon 2005

Track 3: Power and Package Co-Design (3-WP1)

Design of a Low-Power Differential Repeater Using Low-Voltage Swing and Charge Recycling

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Problem Statement

- **Power is the largest problem facing IC/SoC designers**

- **On-chip trace delay limits performance in DSM**

  1) Repeaters are used to reduce delay

  2) Repeaters add power

Agenda

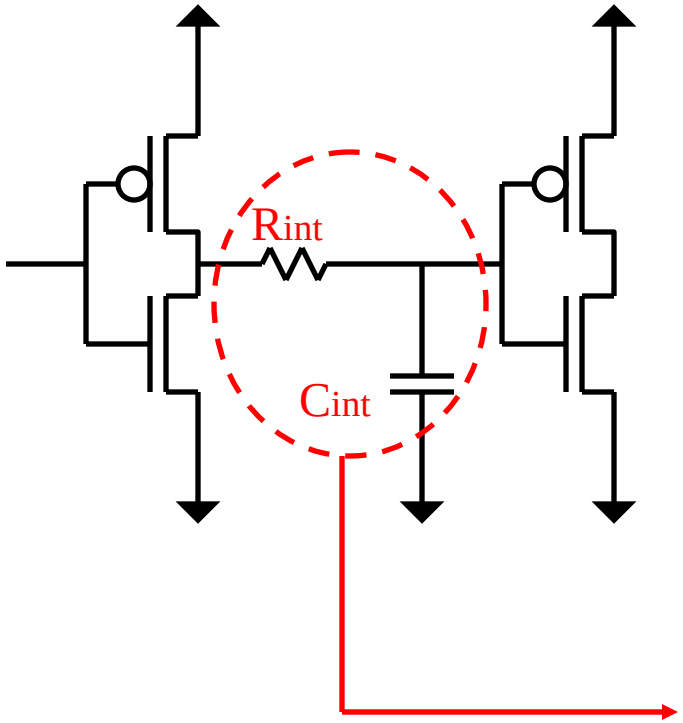
1) Problem Motivation

2) Proposed Solution

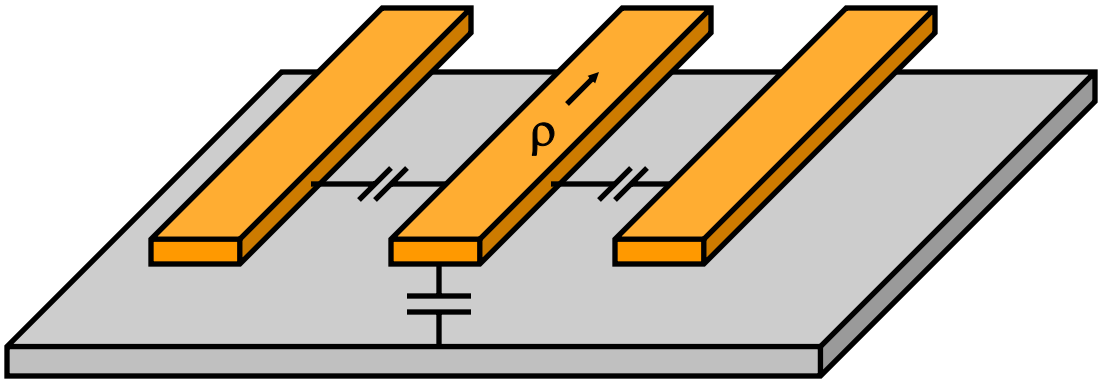
3) Simulation Results

Problem Motivation

RC Trace Delay

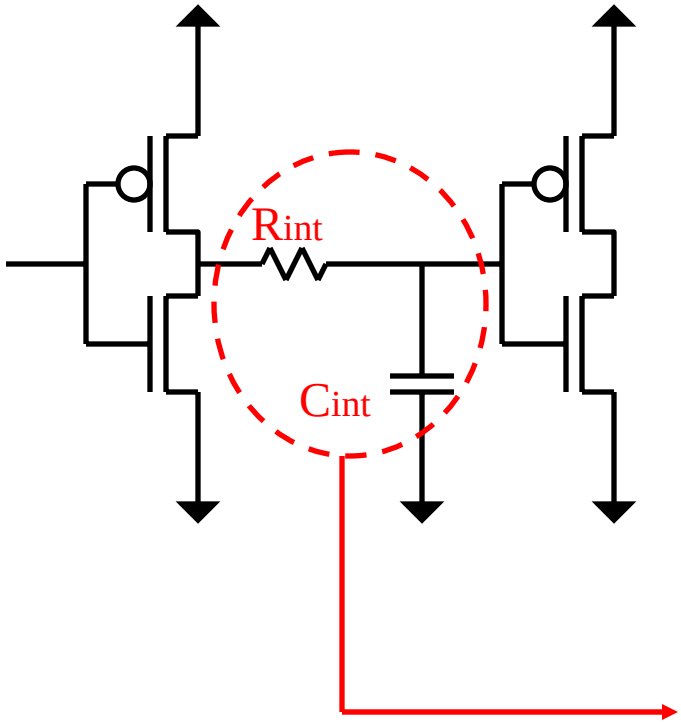


$$t_{RC} = (0.69) \cdot RC$$



Problem Motivation

RC Trace Delay

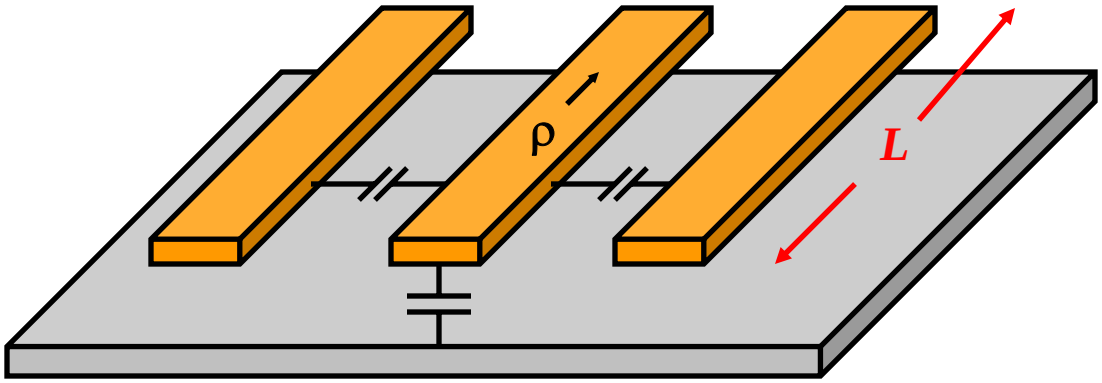


$$R = \frac{\rho L}{A} \propto L$$

$$C = \frac{\varepsilon \cdot W \cdot L}{t_{ox}} \propto L$$

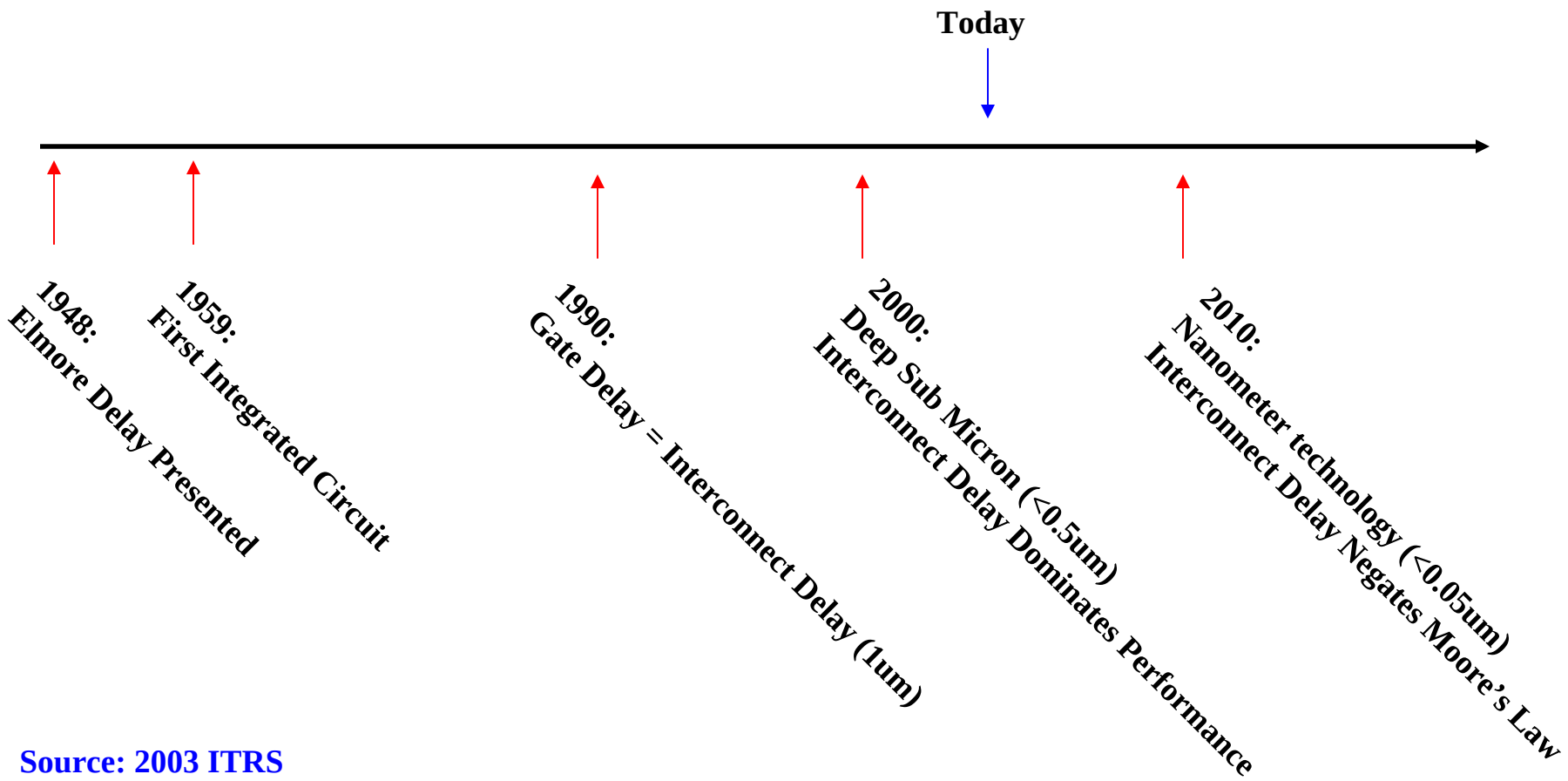
$$t_{RC} \propto L^2$$

Quadratic Increase



Problem Motivation

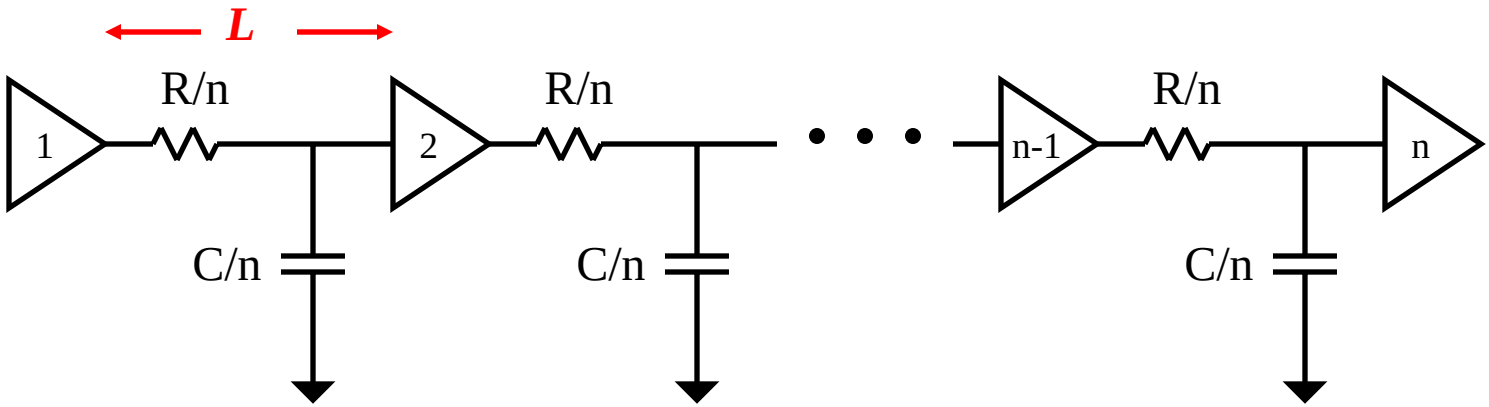
Interconnect Dominates DSM Performance



Source: 2003 ITRS

Problem Motivation

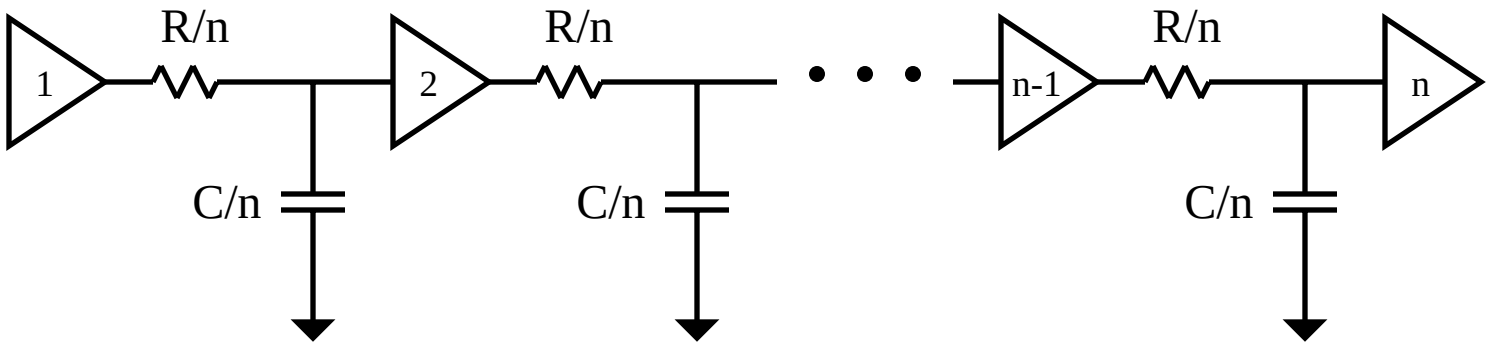
Standard Solution : **"Repeater Insertion"**



- **Break line into smaller segments:** $(L \rightarrow 0)$
- **Optimal sizing when:** $t_{buf} = t_{RC}$
- **Linear dependence:** $t_{delay} \propto L$

Problem Motivation

Repeaters Add Power



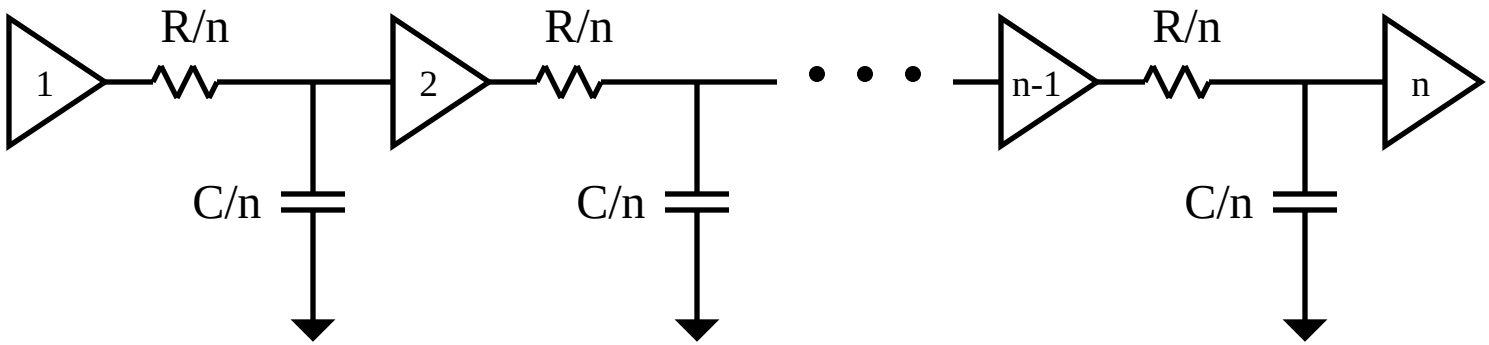
$$P_{dynamic} = C \cdot V_{swing}^2 \cdot f$$

$$P_{short-circuit} = I_{sat} \cdot V_{DD} \cdot f$$

Power $\propto$ (# of Repeaters)

Problem Motivation

Repeater Power Scaling Isn't Realistic

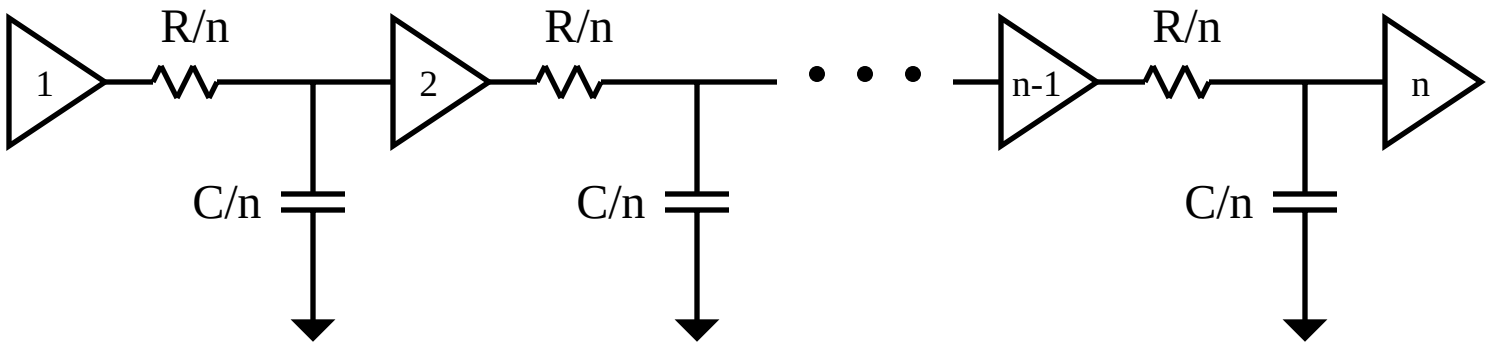


2003 ITRS Prediction:

- **at 50nm, global interconnect will consume 40% of power in VLSI**
- **0.25um *uP* : 50,000 repeaters : 8 Watts**
- **70nm *uP* : 700,000 repeaters : 60 Watts**

Problem Motivation

Need to Reduce Power



- **Need techniques to reduce power of repeater scheme**
- **A small decrease in delay is acceptable**
- **Net improvement in PDP is the goal**

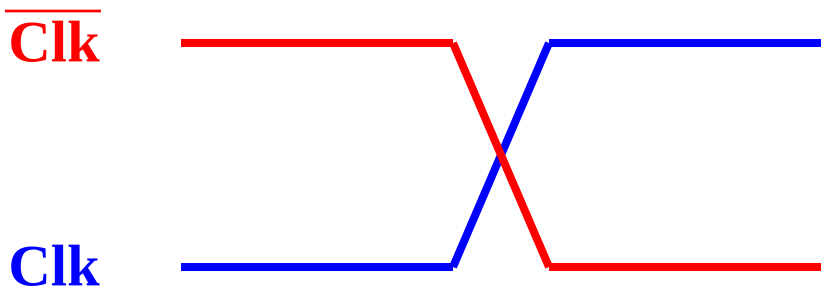
Proposed Solution

Current Trends

- **Differential signaling on clock traces for Noise Immunity**

  - Well Suited for Low-Voltage Output Swing

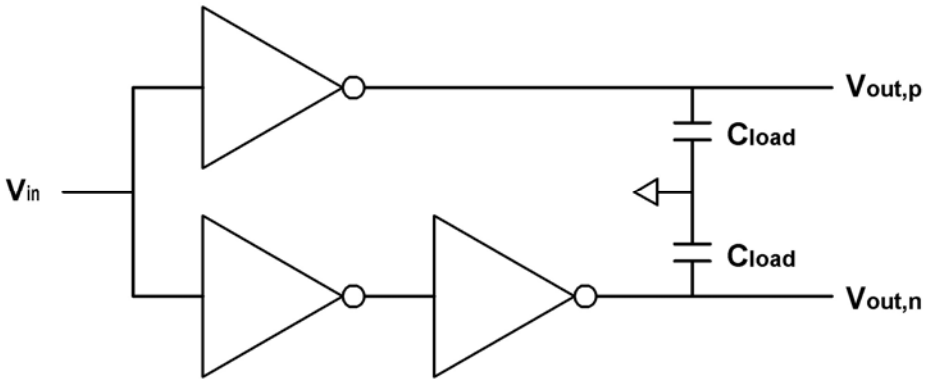
  - Well Suited for Charge Sharing

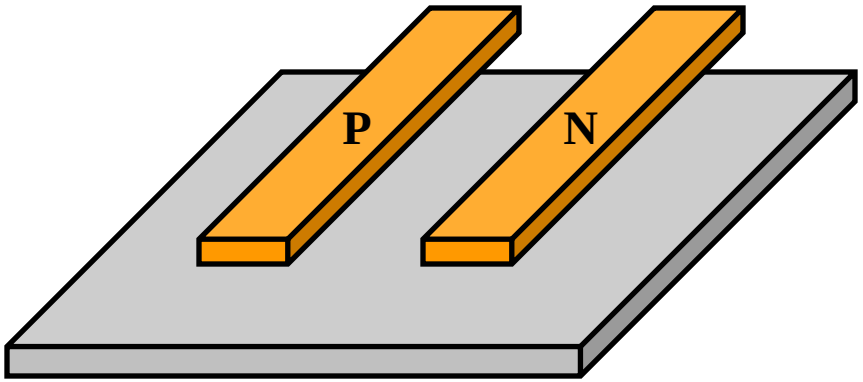


Proposed Solution

Differential Signaling

- **Complimentary Outputs for VLSI CMOS**
- **Receiver Performs (CLK-$\overline{CLK}$) which rejects coupled noise**
- **Receiver Performs (CLK-$\overline{CLK}$) which doubles effective amplitude**





Proposed Solution

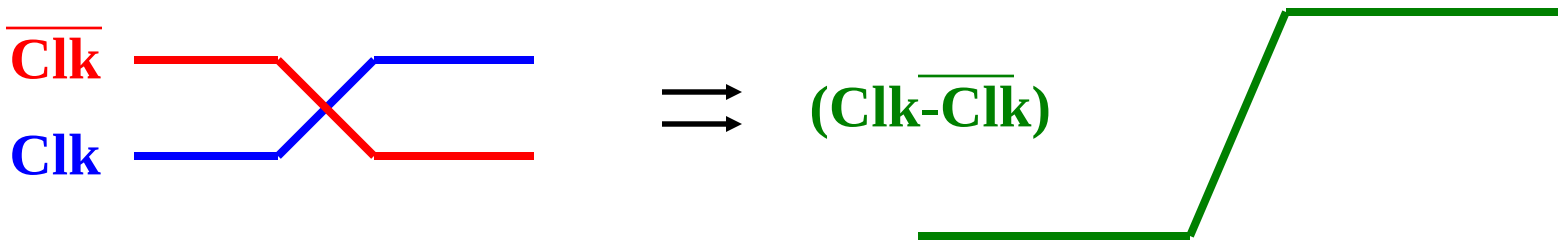
Low-Voltage Swing Outputs

- **Reducing Output Swing Reduces Power**

$$P_{dynamic} = C \cdot V_{swing}^2 \cdot f$$

Quadratic Decrease!!!

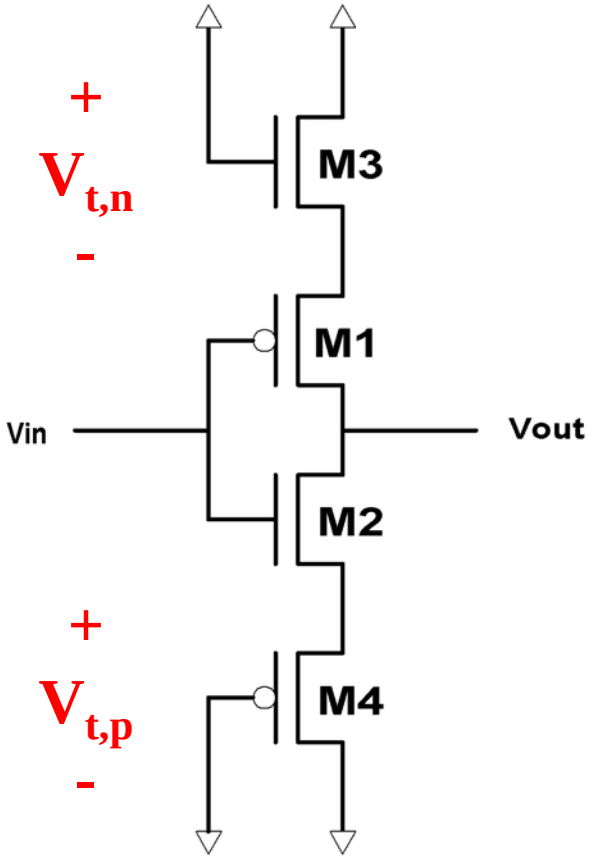
- **Differential Signaling has extra margin to accommodate this**



Proposed Solution

Low-Voltage Swing Outputs

- **Typical CMOS swings from V_{SS} to V_{DD}**
- **Insert V_t drops between supplies to reduce output swing**



Proposed Solution

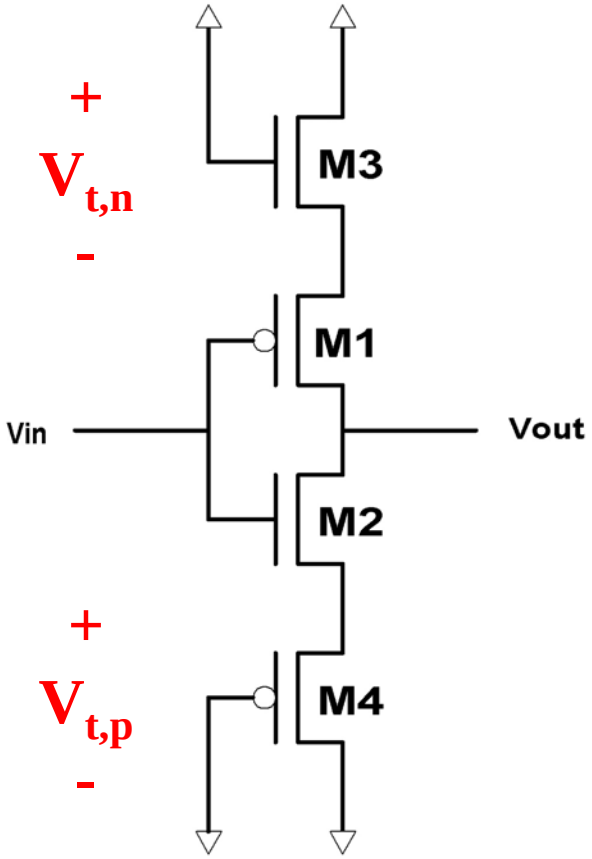
Low-Voltage Swing Outputs

- **The reduced output swing is:**

$$V_{LV-swing} = V_{DD} - V_{t,n} - |V_{t,p}|$$

- **The reduced power is:**

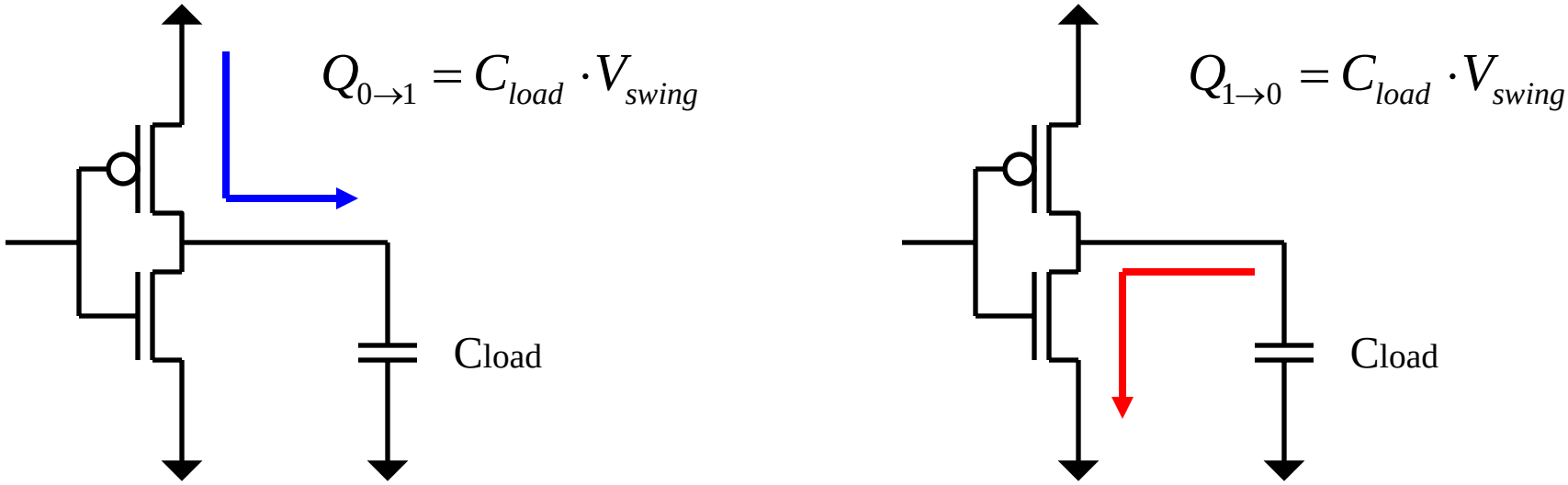
$$P_{dynamic} = C \cdot V_{LV-swing}^2 \cdot f$$



Proposed Solution

Charge Recycling

- **Typical CMOS charges output from supply**



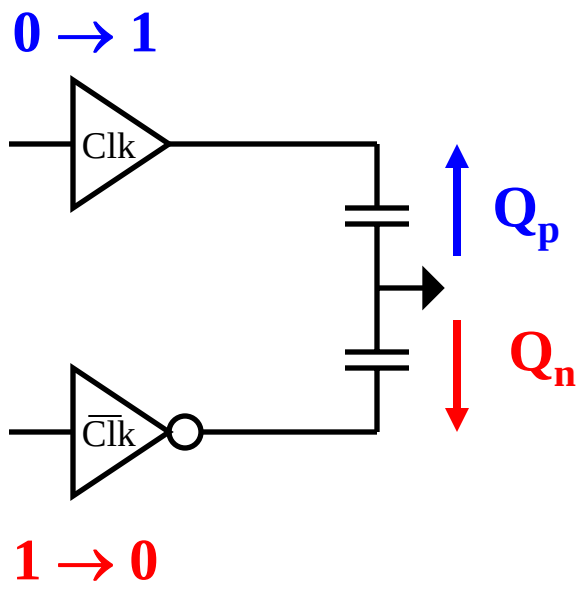
0 → 1 Transition

1 → 0 Transition

Proposed Solution

Charge Recycling

- **The Symmetry of Differential Signaling can be exploited**

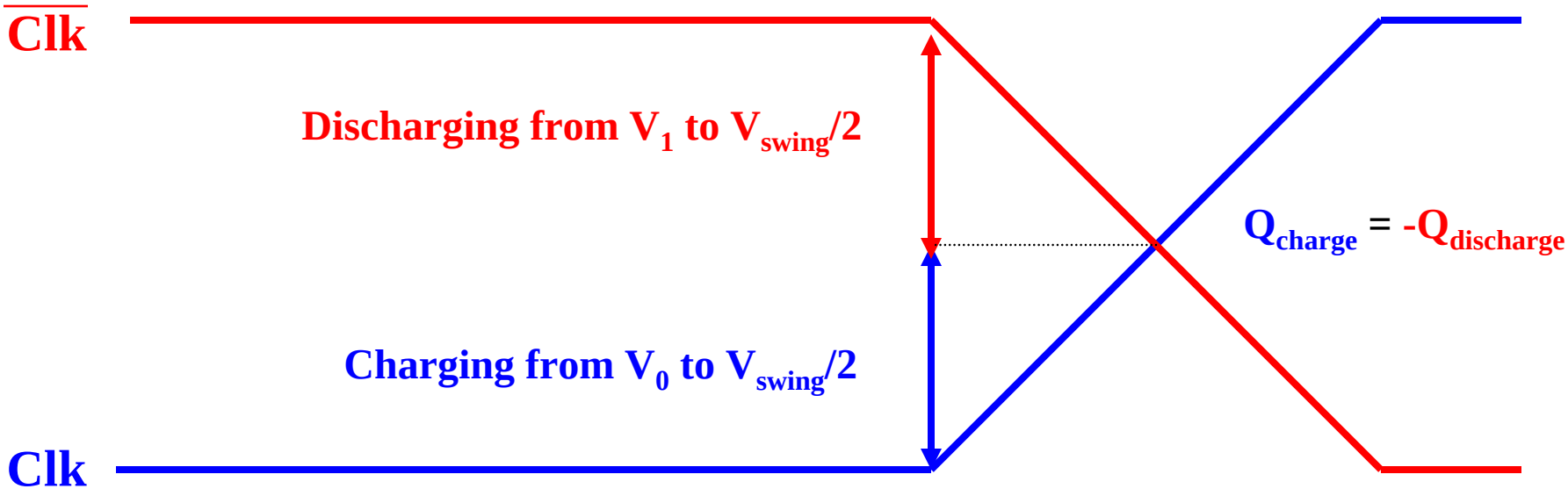


One Driver is always charging while the other is discharging

Proposed Solution

Charge Recycling

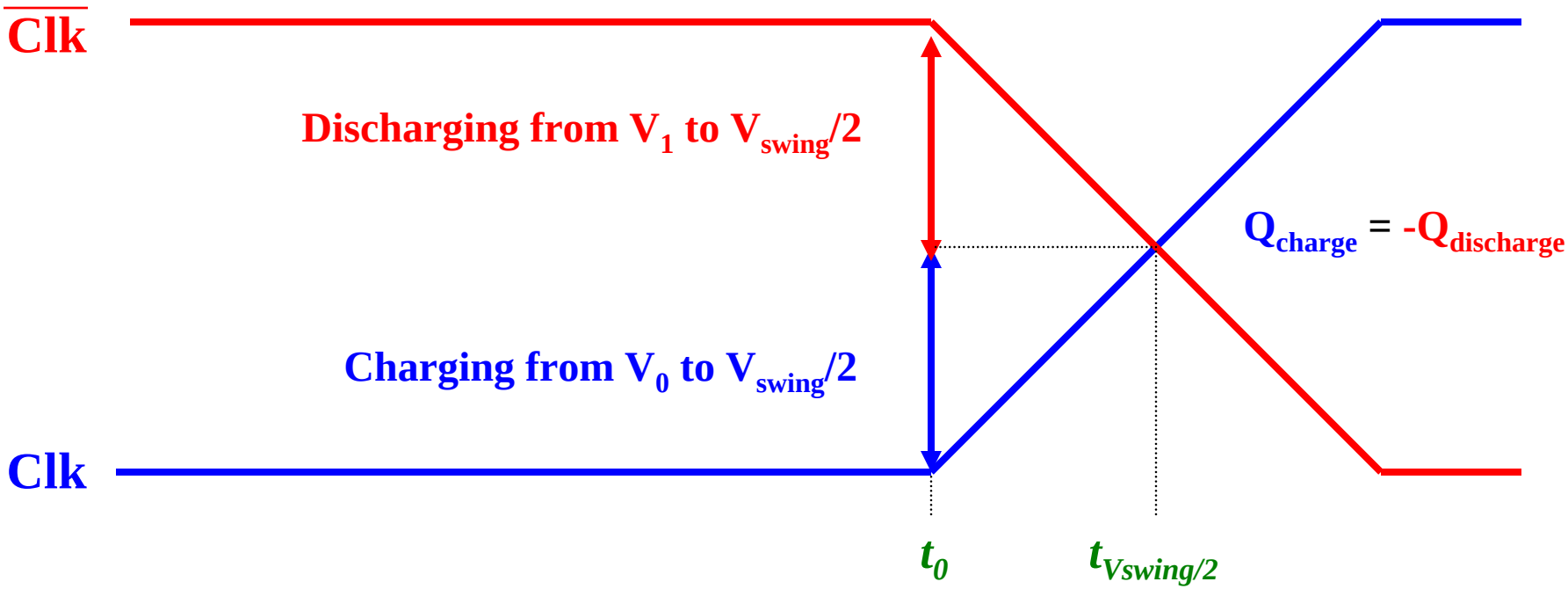
- During first half of the transition equal charge is distributed



Proposed Solution

Charge Recycling

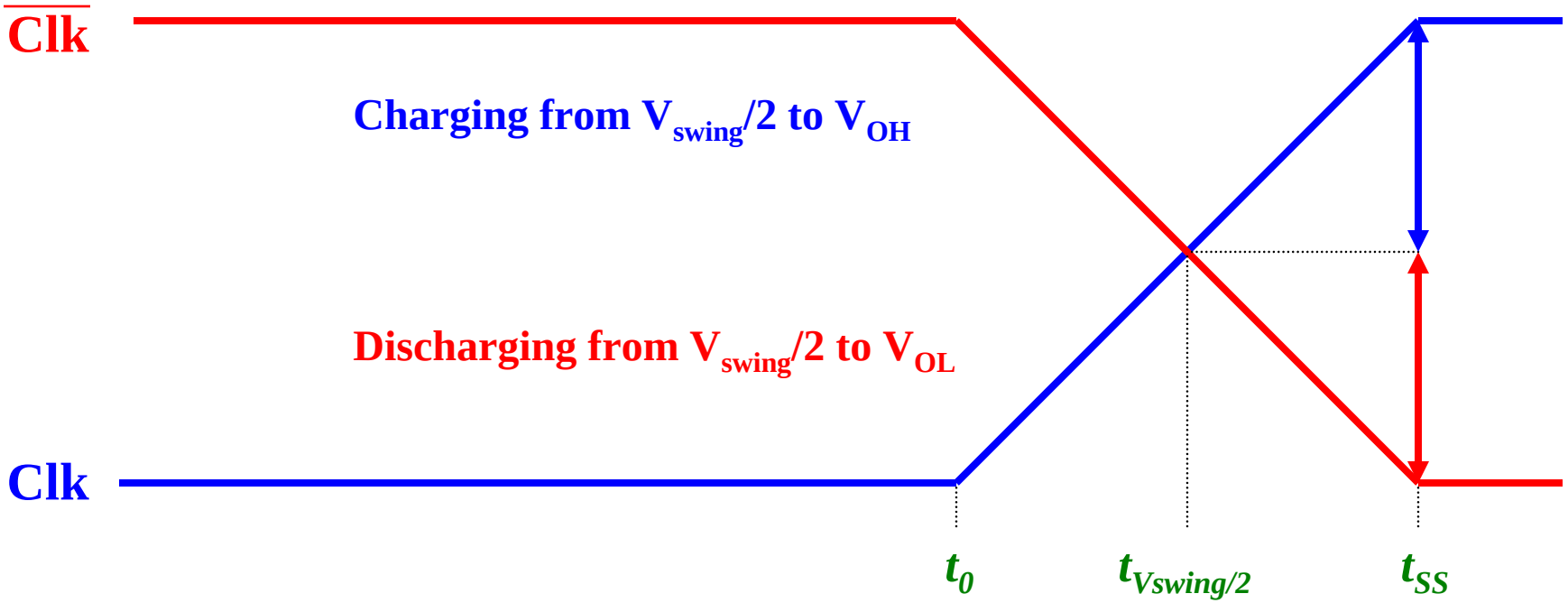
- Charge can be "Shared" between Clk & $\overline{\text{Clk}}$ from t_0 to $t_{Vswing/2}$



Proposed Solution

Charge Recycling

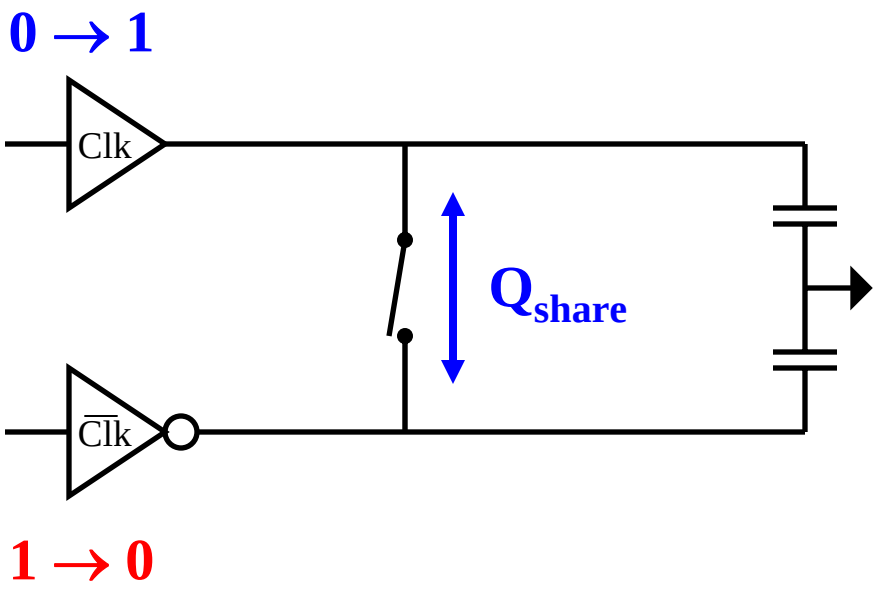
- From $t_{Vswing/2}$ to t_{SS} charge is provided by Supplies as usual



Proposed Solution

Charge Recycling

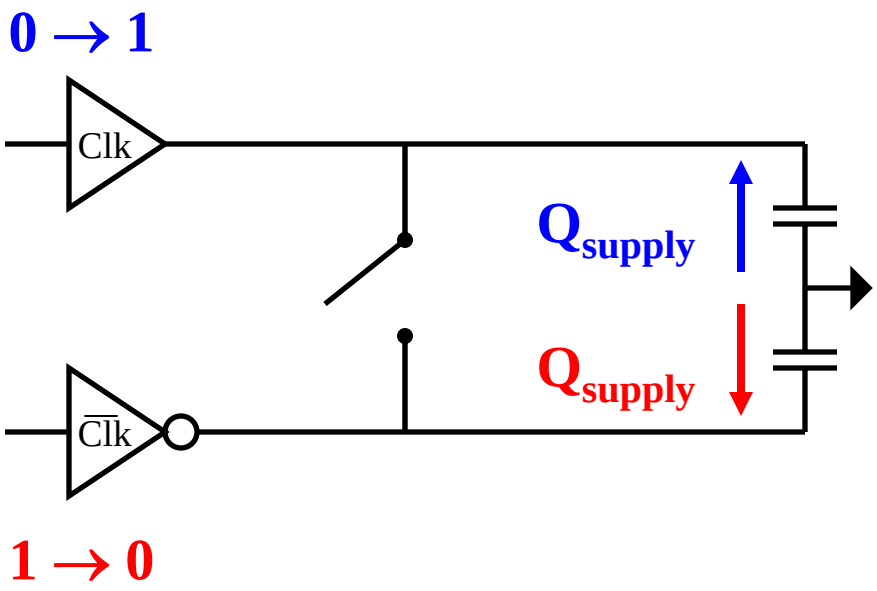
- **Clk & Clk are connected from t_0 to $t_{Vswing/2}$**



Proposed Solution

Charge Recycling

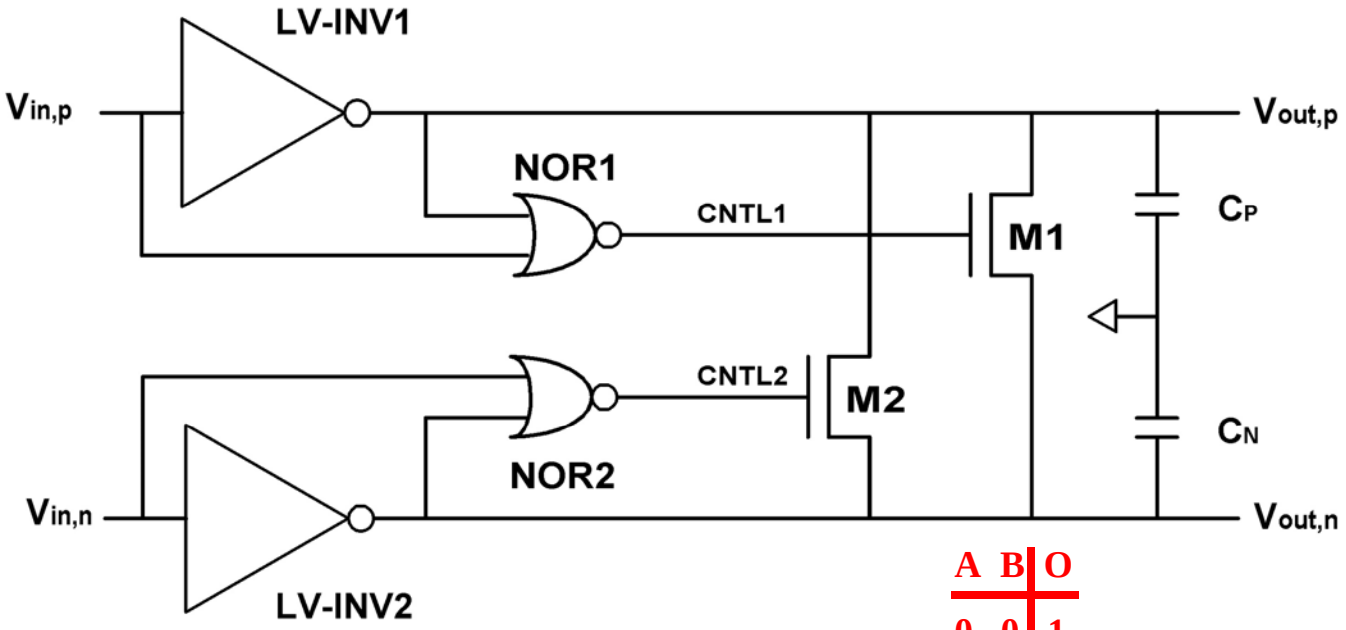
- **Clk & Clk are disconnected from $t_{Vswing/2}$ to t_{SS}**



Proposed Solution

Charge Recycling

- **Circuit Description**

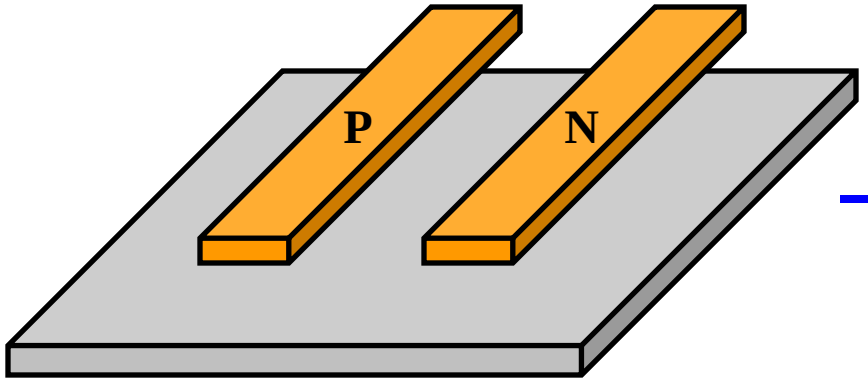


A	B	O
0	0	1
0	1	0
1	0	0
1	1	0

Simulation Results

Trace Modeling

- **BSIM 0.1um Process (BPTM)**
- **1cm Length**
- **Metal 3**

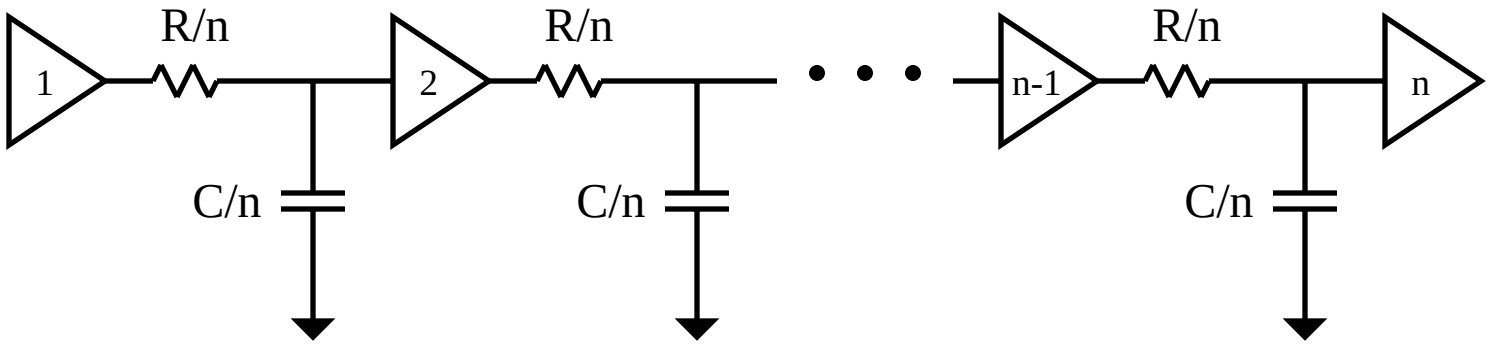


$R_{trace} = 1333\Omega$

$C_{trace} = 1.29pF$

Simulation Results

Repeater Design



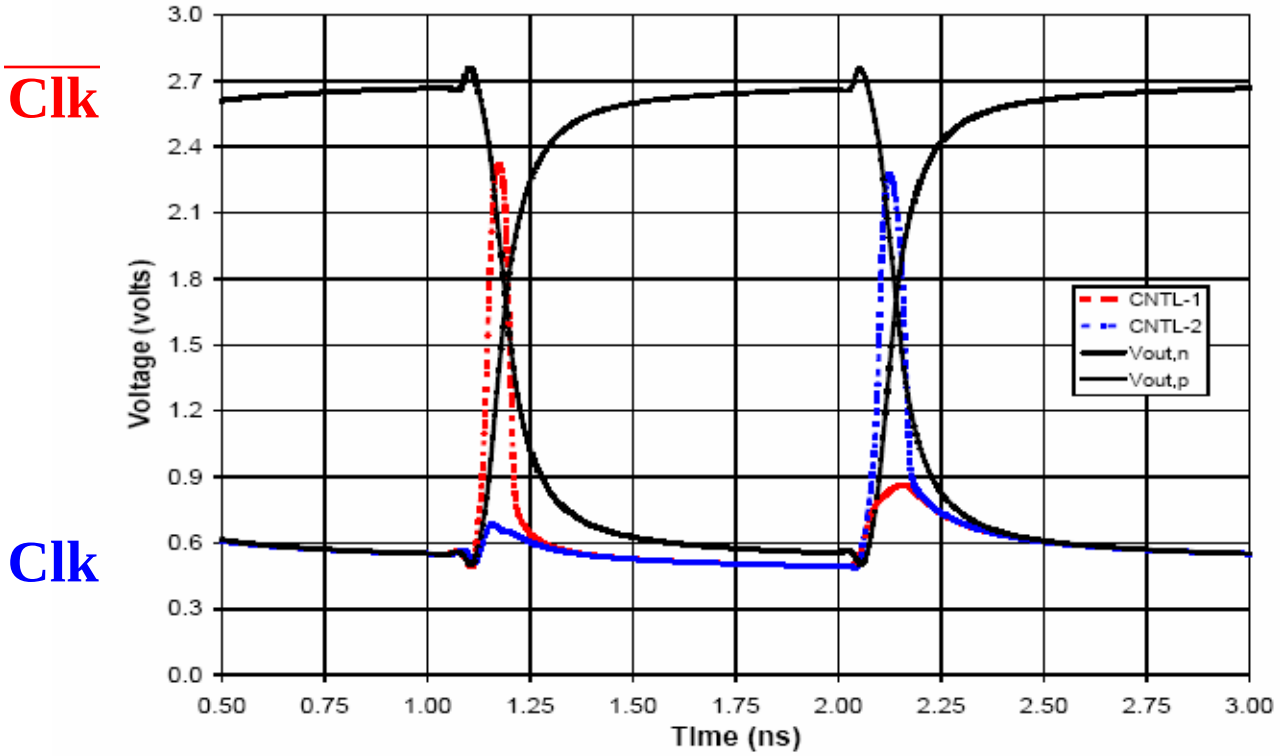
Using Optimal Sizing:

- **Full-Swing Repeater: 15**
- **Low-Voltage Repeater: 9**
- **Low-Voltage Charge Recycling Repeater: 9**

Simulation Results

Circuit Operation

- **Circuit Operation**



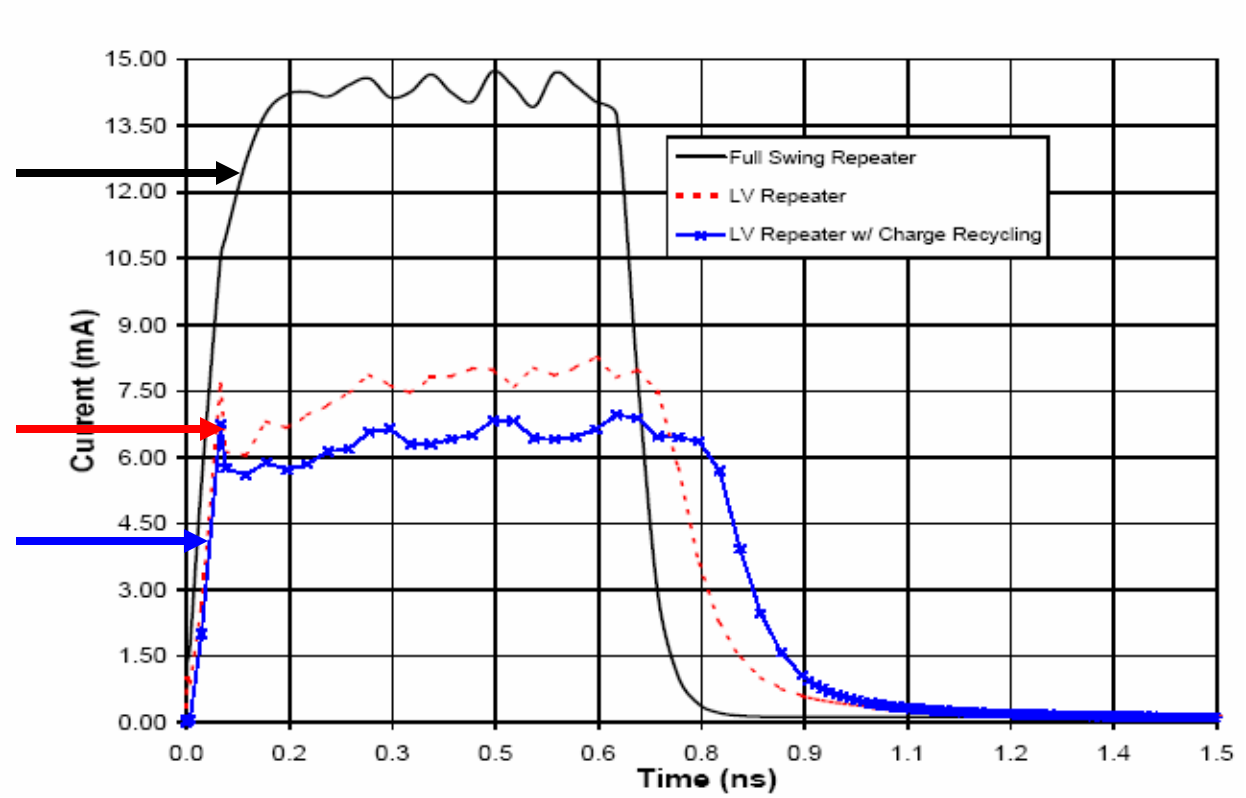
Simulation Results

Current Profile vs. Time

Full-Swing

Low-Voltage

LV Charge-Recycling



Simulation Results

Performance

Both Improve PDP

Circuit	Figures of Merit			Improvement		
	Delay (ps)	Power (mV)	PDP (ps · mV)	Delay (%)	Power (%)	PDP (%)
Full-Swing Repeater	639	12.06	7.71	-	-	-
Low-Voltage Repeater	699	7.54	5.27	-9	37	32
Low-Voltage Charge Recycling Repeater	774	6.92	5.36	-21	43	31

- **Lowest Delay = Full-Swing Repeater**
- **Lowest PDP = Low-Voltage Repeater (32% improvement)**
- **Lowest Power = Low-Voltage Charge Recycling Repeater (43% improvement)**

Implementation Details

Suggested Use

- **On-Chip Metal 3 or Greater**

Not Suggested

- **On-Chip Metal 1 or 2**
  (too much resistance, acts distributed)
- **Off-Chip**
  (too much inductance, acts distributed)

Implementation Details

Sizing

Circuit	Section	Transistor	Size
Full-Swing Repeater	INV	NMOS	2.5/0.1
		PMOS	8.0/0.1
Low-Voltage Repeater	INV	NMOS	5.0/0.1
		PMOS	16.0/0.1
	V_t Drop	NMOS	25/0.1
		PMOS	80/0.1
Low-Voltage Charge Recycling Repeater	INV	NMOS	5.0/0.1
		PMOS	16.0/0.1
	V_t Drop	NMOS	25/0.1
		PMOS	80/0.1
	NOR	NMOS	0.2/0.1
		PMOS	0.8/0.1
	CS	NMOS	0.2/0.1

- Low Resistance
- Negligible Capacitance

< (20%) τ_{load}

Summary

Trends

- **Power and Delay are major problems in DSM**
- **Repeaters are expected to dominate power**
- **Differential signaling is being used for noise immunity on clocks**

Proposed Technique

- **Low-Voltage Swing enabled by differential signaling**
- **Charge Recycling enabled by differential signaling**
- **Suffer small delay penalty for decreased power (PDP ↑)**

Questions?