Power Efficiency Benchmarking of a Partially Reconfigurable, Many-Tile System Implemented on a Xilinx Virtex-6 FPGA

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***Abstract*—Field Programmable Gate Arrays are an attractive platform for reconfigurable computing due to their inherent flexibility and low entry cost relative to custom integrated circuits. With modern programmable devices exploiting the most recent fabrication nodes, designs are able to achieve device-level performance and power efficiency that rivals custom integrated circuits. This paper presents the benchmarking of performance and power efficiency of a variety of standard benchmarks on a Xilinx Virtex-6 75k device using a tiled, partially reconfigurable architecture. The tiled architecture provides the ability to swap in arbitrary processing units in real-time without re-synthesizing the entire design. This has performance advantages by allowing multiple processors and/or hardware accelerators to be brought online as the application requires. This also has power efficiency advantages by keeping unused tiles un-programmed to reduce static power consumption. This paper presents the benchmarking results using a custom Virtex-6 board with a power regulation system that allows instrumentation of each power supply on the Virtex-6 to measure both performance and power efficiency simultaneously.**

Keywords—benchmarking; power efficiency; reconfigurable computing; partial reconfiguration; FPGAs;

I. INTRODUCTION

Field Programmable Gate Arrays (FPGAs) have emerged as the platform of choice for reconfigurable computing due to their design flexibility, real-time reconfiguration and abundant resources. FPGAs have exploited the continual advancement of semiconductor fabrication processing with feature sizes currently as small as 20nm [1]. This has in turn yielded FPGAs with sufficient resources to implement entire many-core computer systems with transistor-level performance (both delay and power efficiency) that is on par with high-end custom integrated circuits (ICs) [2]. FPGAs have also been shown to outperform general purpose processors in many applications by customizing their hardware for the specific application [3-6]. The programmability of FPGAs presents an inherent overhead that has historically caused FPGA-based systems to lag behind the performance of equivalent application specific integrated circuits (ASICs); however, power consumption is now becoming the primary concern of today's ASICs using nanometer process nodes and has stalled the continually increase of clock frequencies. This is making FPGAs more performance competitive with each process node [7].

Power consumption is also a major concern in FPGAs using nanometer process nodes. Great strides have been made in the design of nanometer FPGAs to minimize power consumption. Techniques such as triple oxide, transistor distribution optimization and local suspend circuitry have been implemented in the Xilinx Virtex-6 to address the power consumption concern [8]. One feature that promises to not only increase the performance of FPGA-based system but also reduce power is partial reconfiguration (PR) [9]. Partial reconfiguration is the process of only programming a particular portion of the FPGA during run-time. This has architectural advantages by allowing the same logic to implement different functions at different times. This feature can be exploited to reduce the required size of an FPGA for particular applications by using the same resources sequentially. For systems where having abundant resources available at all times is desired, PR can be used to reduce static power consumption by *un-programming* regions of the FPGA that are not being used [10]. This feature enables dynamic resource scaling as the application requires while saving power when the application does not.

In this paper, a partially reconfigurable, many-tile architecture is presented. In this approach, an FPGA is divided into tiles, each with the characteristic that they can contain a full soft processor or common hardware accelerator and also be partially reconfigured. The tiles are interconnected using a point-to-point parallel IO bus. The system is configured in real-time to match the hardware resources to the requirements of the application while simultaneously saving power by leaving unused tiles un-programmed. Using this approach, a range of hardware architectures can be implemented including a single processor, a hardware accelerated processor, a multi-core system and any combination therein. This architecture is implemented on a Xilinx Virtex-6 75k FPGA with the *MicroBlaze* soft processor [11] as the base processing unit. The Virtex-6 system in this work is able to accommodate nine tiles. A custom Virtex-6 board and a dedicated power regulation system was designed to evaluate the performance of this approach. A Xilinx Spartan-6 is included on the primary FPGA board to facilitate partial reconfiguration of the tiles through the SelectMAP port of the Virtex-6. The power

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regulation system enables the instrumentation of each power rail on the Virtex-6, thus providing a means to isolate the power efficiency of the architecture on the Virtex-6 under a variety of benchmarks. The system was tested using the Dhrystone [12], Whetstone [13], LINPACK [14] and NAS-EP [15] benchmarks. This paper presents the design of the evaluation system and the results of the benchmarks in terms of both performance and power efficiency.

II. System Design

A. FPGA System

A custom board was designed that contained a Xilinx XC6VLX75T FPGA. The Virtex-6 was configured both fully and partially using a separate Xilinx Spartan-6 XC6SLX75. The configuration bit streams for the Virtex-6 were contained on a microSD card. This board is show in Fig. 1.

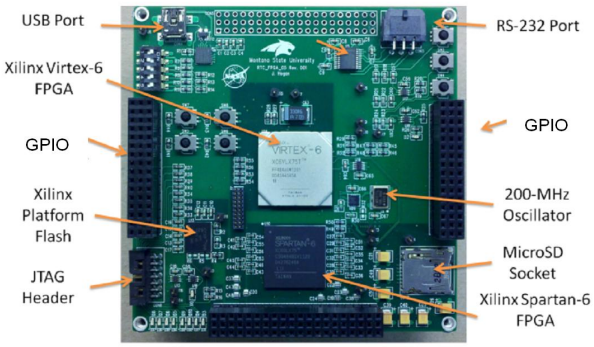

Fig. 1. Custom Virtex-6 Board Developed for the Benchmarking.

The Virtex 75k device was able to contain nine separate tiles, each of which could contain various configurations of the Xilinx MicroBlaze soft processor in addition to the common hardware accelerator cores used in the benchmarks studied. The tile overview and corresponding floor plan of the Virtex-6 is shown in Fig. 2. The highlighted squares in the floor plan represent the partially reconfigurable tiles.

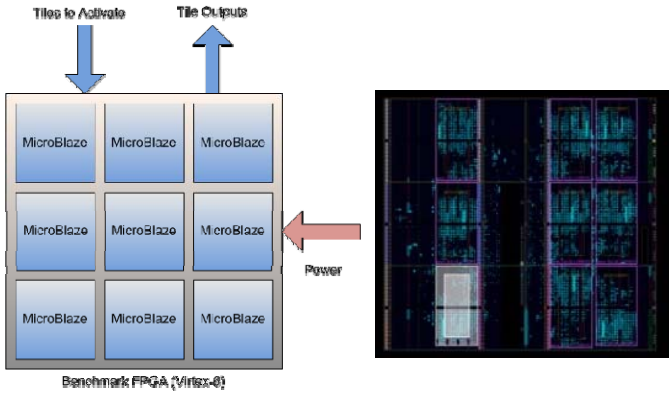

Fig. 2. Floor Plan of the Virtex-6 FPGA Highlighting the 9 Tiles.

B. Power Regulation System

A custom power regulation system was designed to provide the individual voltage rails to the FPGA board. The system is designed to take in a single power supply voltage from +9 to +30 volts and uses a series of Texas Instruments (TI) DC-to-DC converters to step down the voltages for the Virtex-6 and Spartan-6 FPGAs. The voltage distribution network is shown in Fig. 3. Each of the currents in this network are monitored using *Power System Health Monitors* from Texas Instruments. The custom power regulation board is shown in Fig. 4. An example readout from the health monitors is shown in Fig. 5.

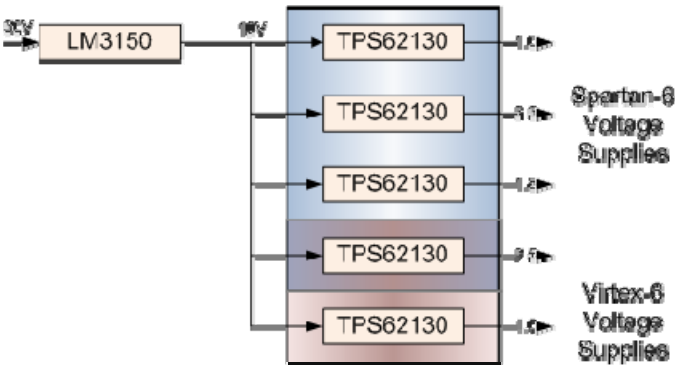

Fig. 3. Example of a figure caption. (*figure caption*)

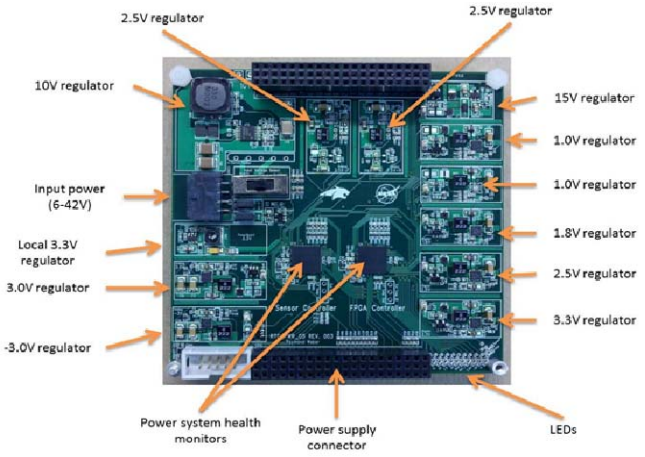

Fig. 4. Custom Power Regulation Board Developed for the Benchmarking.

Fig. 5. Exampel Readout from the Texas Instrument Power System Health Monitors.

III. BENCHMARKING RESULTS

Table 1. gives the performance benchmark results for the Dhrystone, Whetstone and LINPACK benchmarks. In this table, the Virtex-6 system clock frequency was 120 MHz. The Dhrystone benchmark (v2.1) performs all of its operations using integer data types (32-bit). The MicroBlaze processor contains hardware ALU support for 32-bit integer arithmetic operations so no addition acceleration is necessary, thus the benchmarking was performed using a single-core configuration. The Whetstone benchmark performs its operations on single-precision floating point data types (32-bit). Again, the MicroBlaze processor contains hardware ALU support for 32-bit single-precision arithmetic operations so no addition acceleration is necessary and the benchmarking was completed using a single-core configuration. The LINPACK benchmark can be performed using both single-precision and double precision (64-bit) operations. For the LINPACK single-precision, a single-core MicroBlaze was used. For the LINPACK double-precision operations, an additional 64-bit floating point processing unit (FPU) was added to the MicroBlaze since a 64-bit FPU is not built in. This 64-bit FPU was included as part of the MicroBlaze so the system still resided within a single-tile.

TABLE I. BENCHMARK PERFORMANCE RESULTS FOR DHRYSTONE, WHETSTONE AND LINPACK WITH A SYSTEM CLOCK OF 120MHZ

Benchmark	FPGA Tile Configuration	
	Single Core	Single Core with Floating Point Hardware Accelerator
Dhrystone	122 DMIPS	n/a
Whetstone (single precision)	6.3 MFLOPS	n/a
LINPACK (single precision)	11.3 MFLOPS	n/a
LINPACK (double precision)	0.31 MFLOPS	1.9 MFLOPS

Table 2. gives the performance benchmark results for the Dhrystone, Whetstone and LINPACK benchmarks normalized to a clock frequency of 1MHz. This is often a better measure of performance between computer architectures since clock rates can vary significantly across platforms for a variety of reasons not directly related to the architecture of the computer. The Dhrystone performance of 1.01 DMIPS/MHz compares favorably to the published Xilinx theoretical performance for the MicroBlaze of 1.3 DMIPS/Mhz [16]. It is anticipated that with further place and route manipulation, the Virtex-6 system in our work could achieve this theoretical maximum. The performance of the single-precision versions of Whetstone and LINPACK also match similar studies using the MicroBlaze soft processor [17, 18] with slight differences again being attributed to place and route optimization. Adding a 64-bit FPU accelerator improved performance of the double-precision LINPACK benchmark by over 500% on our system.

TABLE II. BENCHMARK PERFORMANCE RESULTS FOR DHRYSTONE, WHETSTONE AND LINPACK NORMALIZED TO A SYSTEM CLOCK OF 1MHZ

Benchmark	FPGA Tile Configuration	
	Single Core	Single Core with Floating Point Hardware Accelerator
Dhrystone	1.01 DMIPS/MHz	n/a
Whetstone (single precision)	52.5 KFLOPS/MHz	n/a
LINPACK (single precision)	94.2 KFLOPS/MHz	n/a
LINPACK (double precision)	2.9 KFLOPS/MHz	15.8 KFLOPS/MHz

Table III. gives the power efficiency results for the Dhrystone, Whetstone and LINPACK benchmarks. These power efficiencies were collected at a system clock rate of 120MHz. Running a single-core system on the Virtex-6 FPGA with the remaining 8 tiles left un-programmed consumed a total of 610mW. The addition of the 64-bit FPU added an additional 1mW.

TABLE III. BENCHMARK POWER EFFICIENCY FOR DHRYSTONE, WHETSTONE AND LINPACK WITH A SYSTEM CLOCK OF 120 MHZ

Benchmark	FPGA Tile Configuration	
	Single Core	Single Core with Floating Point Hardware Accelerator
Dhrystone	200 DMIPS/Watt	n/a
Whetstone (single precision)	10.3 MFLOPS/Watt	n/a
LINPACK (single precision)	18.5 MFLOPS/Watt	n/a
LINPACK (double precision)	0.51 MFLOPS/Watt	3.1 MFLOPS/Watt

The NAS Parallel benchmark was created to stress highly parallel supercomputers. It allows incremental processors to be brought online without a significant inter-core communication overhead. The NAS benchmark is not specified in instructions-per-second but rather in the time it takes to complete a set of computation iterations. Our system was benchmarked using the NAS-EP Kernel for 2^{20} iterations up to a 5 core system. The results are given in Table IV. For each configuration, the total amount of Virtex-6 power is given. This table illustrates that this algorithm has an extremely low overhead associated with bringing on more cores for computation and is only representative for applications that can be parallelized with minimal core-to-core interaction. The power consumption for incremental cores being brought online is minimal compared to the increase in computation that is achieved. The majority of the power is consumed in the single-core system. It is suspected that this power is due to the global FPGA requirements (e.g., configuration memory, clock and reset routing) and the point-to-point routing network of the many-tile architecture.

TABLE IV. BENCHMARK PERFORMANCE RESULTS FOR NAS-EP WITH A SYSTEM CLOCK OF 120MHZ

FPGA Tile Configuration	Results (2^{20} Iterations)			
	Completion Time	Speed Up Over 1 Core	Power Consumption	Power Increase Over 1 Core
1 Core	393 s	-	610mW	-
2 Cores	195 s	202%	618mW	1.3%
3 Cores	131 s	300%	626mW	2.6%
4 Cores	97 s	405%	634mW	3.9%
5 Cores	77 s	501%	642mW	5.2%

IV. BENCHMARKING RESULTS

This paper presented the benchmarking of performance and power efficiency of a many-tile, partially reconfigurable computer system implemented on a Xilinx Virtex-6 FPGA using the MicroBlaze soft processor. For the Dhrystone, Whetstone, LINPACK and NAS-EP benchmarks, the MicroBlaze produced performance results that matched expectations when the clock frequency was normalized. The power efficiency was measured for these benchmarks simultaneously. It was shown that brining on additional computation cores only used an incremental 8mW. It was also shown that this power could be saved by keeping unused tiles un-programmed.

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