

**CHARACTERIZATION OF A PRINTED
CIRCUIT BOARD VIA**

by

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B.S.E.E., Montana State University, 1998

Technical Report EAS_ECE_2000_09

A thesis submitted to the Graduate Faculty of the

University of Colorado at Colorado Springs

in partial fulfillment of the

requirements for the degree of

Master of Science

Department of Electrical and Computer Engineering

2000

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Characterization of a Printed Circuit Board Via

Thesis directed by Professor T.S. Kalkur, Ph.D.

This paper describes the characterization of a printed circuit board via connecting two semi-infinitely long microstrip transmission lines above a ground plane. An equivalent circuit is developed to fully characterize the via. The equivalent circuit is given consisting of excess capacitance and excess inductance. 3D electromagnetic field simulations are ran to extract the capacitance and inductance from the three-dimensional via model. The simulations consider the effect of pad, cylinder, and ground plane clearance radius. A time-domain analysis is done on a test printed circuit board containing vias of various geometry's using Time Domain Reflectometry. The responses of the test vias are extracted and compared to the simulation results. A full-wave analysis of the test printed circuit board is also done to extract scattering parameters in order to compare the empirical results to the simulations in the frequency domain. Finally design guidelines are given in order to minimize discontinuities by matching the effective characteristic impedance of the printed circuit board via to the microstrip transmission lines.

Acknowledgements

The research in this thesis would not have been possible without the co-sponsorship of **Agilent Technologies** and **Hadco**. *Agilent Technologies* is a worldwide leader in the creation of test and measurement equipment. Through funding and donation of use of test equipment, it was possible to empirically verify ideas presented in this paper. *Hadco* is a manufacturer of controlled impedance printed circuit boards. Without *Hadco*'s funding and ability to create high-speed controlled impedance printed circuit boards at a reasonable cost, empirical measurements of actual *vias* would not have been possible.

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CHAPTER I

INTRODUCTION

Minimizing discontinuities in high-speed controlled impedance transport systems is of considerable importance to the functionality of that system. Excess capacitance and inductance on a transmission line can lead to reflections, signal speed degradation, and unexpected switching in digital circuits. One such discontinuity that is common in multi-layered printed circuit boards is the *via*. The accurate characterization of a printed circuit board via is an important issue in the successful design of high-speed circuits implemented on multi-layered printed circuit boards.

A printed circuit board via is a structure that connects two transmission lines on different layers of a multi-layered printed circuit board. A via consists of a hole drilled through a printed circuit board and plated with a conducting material. This plated hole is referred to as the *cylinder* in this paper. On each layer on which a transmission line is connected to the cylinder, a circular *pad* of conducting material is placed about the cylinder. These pads provide contacts for the transmission lines. In most high-speed circuit boards, the cylinder of the via passes through at least one ground plane. A clearance hole in the ground plane is left so that the cylinder can pass without making contact. Figure 1 shows a three-dimensional cross section of two microstrip transmission lines that connect to a via that passes through one ground plane. The three parameters that this paper investigates are marked on the figure. The three parameters are the radius of the *pad*, *cylinder*, and *ground-clearance*. Figure 2 shows the cross-section of an actual printed circuit board via.

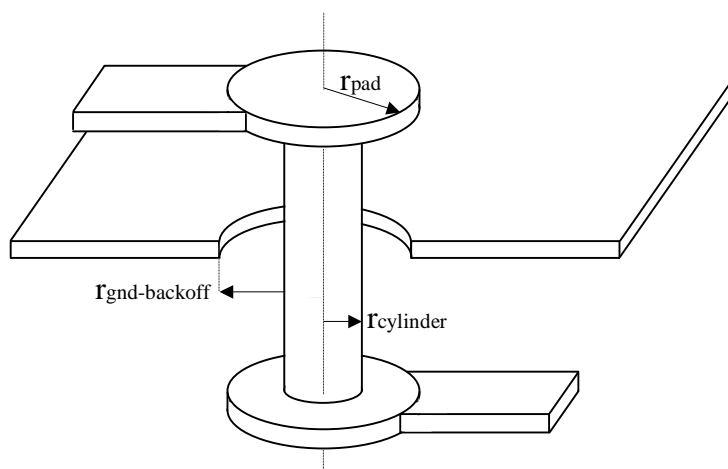


Figure 1. A Via Connecting Two Microstrip Transmission Lines

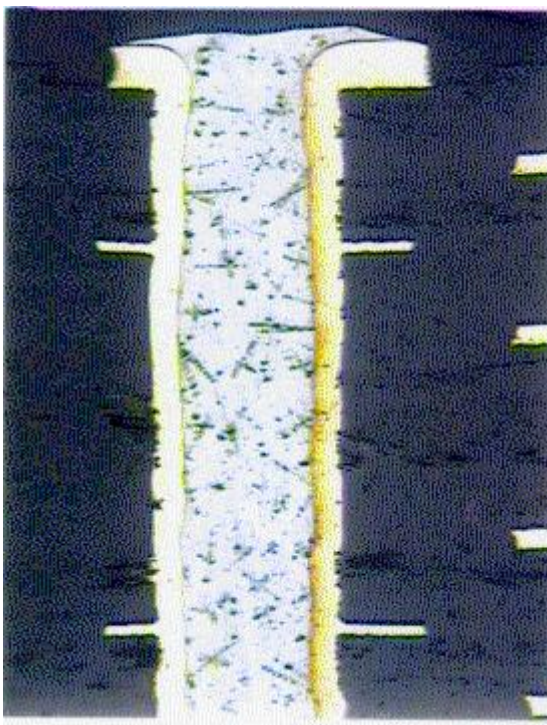


Figure 2. Cross-Section of an Actual Printed Circuit Board Via

The electrical model of a via can be broken into three sections, the upper pad, cylinder, and lower pad. Each section consists of a capacitance and inductance. This paper investigates the impact of the physical geometry of a via and its effect on signal integrity as signals propagate through it. The degradation of signal integrity is a result of parasitic excess capacitance and excess inductance. The term *excess* refers to any additional capacitance or inductance that results in a via's characteristic impedance not matching the characteristic impedance of the connecting transmission lines. Since it has been shown that the worst case parasitics are present when looking at a via without any connections [4], this paper will examine only the stand alone via and adopt it as an upper bound for all other cases. This paper will also limit its investigation to the connection of microstrip transmission lines to the via. The effects on the capacitance and inductance of the via will be studied as its physical geometry is altered. Specifically, capacitance and inductance will be monitored as the radius of the pad, cylinder, and ground-backoff are varied.

An equivalent circuit for the via is developed that can accurately model its electrical response. The physical parameters of the via will be varied in the 3D EM simulations and empirical measurements to show that the equivalent circuit accurately tracks the electrical response over different geometry's.

The change in electrical parameters will be monitored in three ways. First, 3D electromagnetic field simulations will be ran to extract the excess capacitance and inductance of the via. Second, Time Domain Reflectometry measurements will be made on a test circuit board containing vias of various geometry's and the electrical response will be monitored in the time domain. Additionally, scattering parameter

measurements will be taken on the test PCB and the electrical response will be monitored in the frequency domain. The results of all methods will be compared and differences will be discussed. Finally, design guidelines will be given for how to minimize discontinuities by choosing a particular via geometry.

The next section gives a background for the techniques used in this investigation.

CHAPTER II

BACKGROUND INFORMATION

Characteristic Impedance

The goal of a transmission line transport system is to deliver an electrical signal to a specific point without the addition of any distortion or dispersion to that signal. As long as the characteristic impedance, Z_o , of the transmission line is constant at every point throughout the length of the line, the signal will be delivered in tact. When areas of a transmission line have a different Z_o than the rest of the line, reflections will occur. The measure of how much of the incident signal is reflected is defined as Γ , (Gamma, the reflection coefficient). The definition of Γ is as follows [22]:

$$\Gamma = \frac{Z_L - Z_o}{Z_L + Z_o} \quad \text{(Eq. 1)}$$

Z_o in this expression is the characteristic impedance of the transmission line that is used to transmit the signal. Z_L in this expression is the impedance of the load to where the signal is being delivered (or the impedance of the element immediately in front of the signal). The expression for the amount of the signal that is reflected is defined as follows [22]:

$$V_{REFLECTED} = \Gamma \cdot V_{INCIDENT} \quad \text{(Eq. 2)}$$

This expression illustrates that when the impedance of the load matches the impedance of the transport system, Γ will be zero and the entire signal will be

delivered. This paper will only consider *lossless* transmission lines. For a *lossless* transmission line, the characteristic impedance is defined as follows [22]:

$$Z_o = \sqrt{\frac{L}{C}} \quad (\text{Eq. 3})$$

Transmission lines on multi-layered printed circuit boards often need to change signal layers. This is accomplished using a *via*. The *via* is a source of mismatched impedance and can lead to reflections of the incident signal. This paper examines the effect of the physical geometry of a *via* on its electrical parameters C and L. By accurately modeling the effect of the *via*'s physical geometry on its electrical parameters, the effective characteristic impedance of the *via* can be matched to the transmission lines that connect to it, thus eliminating reflection and allowing the entire signal to pass.

3D Electromagnetic Field Simulators

The electrical parameters of a *via* are extracted using a 3D electromagnetic field simulator. The simulator allows physical geometry's to be described, (pad, cylinder, ground plane, etc...) and then solves for the capacitance and inductance at any point or between any two conductors. The simulator used in this paper is the *Avant! Raphael 3D Field Simulator*.

Capacitance and Inductance are extracted by solving Poisson's equation. It is based on the finite difference method with an automatically adjustable rectangular mesh. The linear equations set up by the finite-difference method are solved by the

Incomplete Cholesky Conjugate Gradient method (ICCG). The combination of the automatic adjustment of mesh and the speed of ICCG makes the capacitance and inductance extraction very versatile [23].

Time Domain Reflectometry

A Time Domain Reflectometer (TDR) is a device that sends a step-shaped pulse down a transmission line and concurrently measures the reflected waveform. By monitoring the incident wave and the reflected wave, it is able to determine the characteristic impedance of any point on the line. The measurement is done in the time domain so discontinuities can be isolated from each other with respect to time.

This paper uses TDR measurements on a test circuit board in order to compare the EM simulation results with empirical data in order to verify the accuracy of the equivalent circuit in the time domain. The instrument used to accomplish this is the *Hewlett-Packard 54120A TDR Oscilloscope*.

Network Analysis

A Network Analyzer is a device that sweeps the frequency of a sinusoidal waveform as it enters into a *device under test* (DUT). The network analyzer has two detection devices. The first detection device located at the input to the DUT, measures the reflected voltage. A second detection device is located at the output of the DUT and measures the transmitted voltage. By knowing the incident voltage, the network analyzer can produce measurements known as *S-parameters*, which can fully

characterize a DUT by finding its frequency response. The following two parameters are considered in this paper:

$$S_{11} = \frac{V_{REFLECTED}}{V_{INCIDENT}} = \Gamma \quad \text{(Eq. 4)}$$

$$S_{21} = \frac{V_{TRANSMITTED}}{V_{INCIDENT}} = T \quad \text{(Eq. 5)}$$

Where Γ is the *Reflection Coefficient* and T is the *Transmission Coefficient*. By extracting these two parameters, the response of an element can be determined.

This paper uses measurements taken using a Network Analyzer on a test printed circuit board in order to compare the EM simulation results with empirical data to verify the accuracy of the equivalent circuit in the frequency domain. The instrument used to accomplish this is the *Hewlett-Packard 8753ES Network Analyzer and S-Parameter Test Set*.

CHAPTER III

CHARACTERIZATION APPROACH

This paper develops an equivalent circuit that can accurately model a printed circuit board via. This is accomplished by examining various equivalent circuits and selecting one that can effectively mimic the electrical response of a via while also being practical enough to be used in a development process. Simplifications can be made by limiting the bandwidth for which the via model is accurate for. The next chapter describes the selection of the appropriate equivalent circuit.

Once an equivalent circuit is defined, the electrical parameters (C and L) must be extracted. This is done using a three-dimensional electromagnetic field simulator. Simulations are ran to extract the excess capacitance and inductance from the physical geometry of the via as its geometric parameters are swept, (i.e., pad radius, cylinder radius, ground clearance radius). From these simulations it can be demonstrated how the geometric parameters effect the via's electrical response. Chapter 5 shows the 3D EM simulation results.

To verify that the equivalent circuit and electrical parameter extraction is accurate enough to model the via, empirical measurements must be made. A test printed circuit board was developed which consisted of microstrip transmission lines connecting to vias of different physical geometry's. Measurements were made in both the time domain and frequency domain to ensure that the via model is robust.

Time Domain Reflectometry (TDR) is used to examine the electrical response of the vias on the test printed circuit board. By building a SPICE simulation that accurately mimics the TDR measurement, the 3D EM Field simulation results can be

compared to the empirical results in the time domain. Chapter 6 shows the TDR measurements made on the test printed circuit board.

In the frequency domain, measurements are made on the test printed circuit board using a Network Analyzer. By extracting the *S-parameters* from the frequency response of the test printed circuit board, results can be imported into a SPICE simulation to compare simulation results to empirical data in the frequency domain. Chapter 7 shows the frequency domain measurement results.

Chapter 8 compares the results of all modeling methods to ensure the validity of the equivalent circuit and the characterization approach.

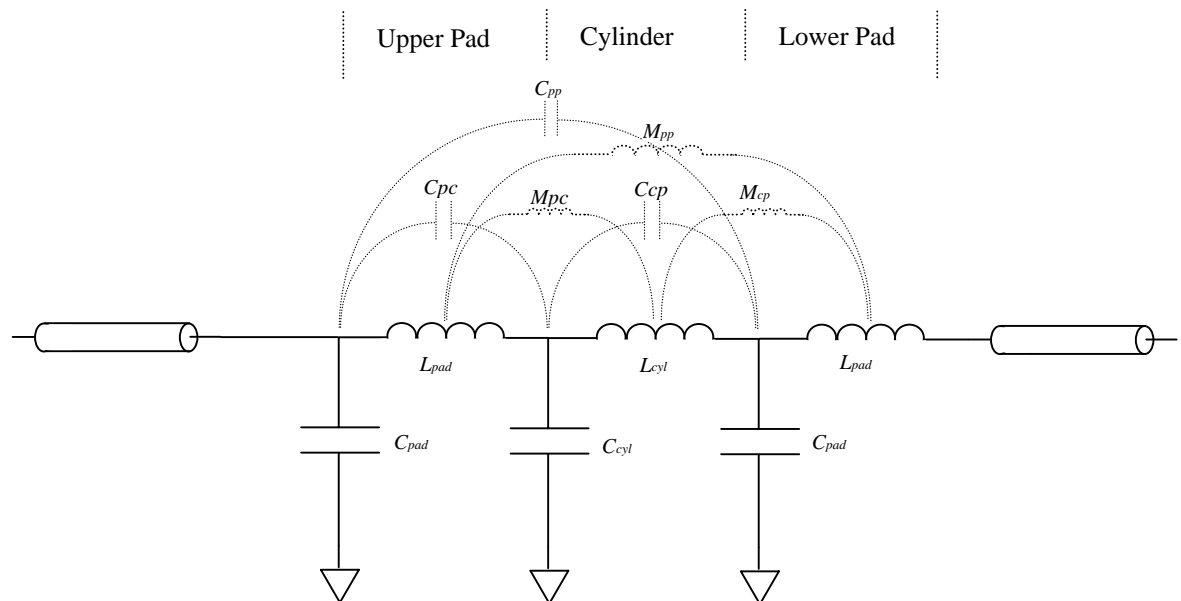
The next chapter examines the selection of an equivalent circuit to accurately model the electrical response of the via.

CHAPTER IV

EQUIVALENT CIRCUIT

To fully characterize the electrical response of a via, an equivalent circuit must be developed. The circuit must be able to accurately model the response while still being practical enough to be used in a development process. The complexity of the equivalent circuit can be reduced by limiting the bandwidth for which the equivalent circuit is accurate for. This chapter will examine three equivalent circuits and describe the selection process

The first circuit shown in figure 3 is the most accurate and complex circuit to describe the microstrip via.



**Figure 3. Via Equivalent Circuit
(Coupled)**

This circuit consists of a traditional distributed 3-element lossless transmission line model. Each element represents the three series sections of the via that the signal passes through, the upper pad, cylinder, and the lower pad. In addition, the coupling between each component is shown. There are mutual capacitances between each of the three main capacitive elements. The three main capacitances are defined as the capacitance to ground between the conducting via segment and the infinite ground plane. The mutual capacitances are present due to the coupling between each of the conducting elements. The 3D electromagnetic field simulations are capable of determining the coupling capacitance.

This circuit also shows the coupling between the inductive elements in the form of *Mutual Inductance*, M . Mutual Inductance is present anytime a changing magnetic field creates a magnetic flux that is coupled onto another near-by conductor in the form of a voltage. This phenomenon is due to *Faraday's Law* which states that a voltage can be induced in a conductor due to an external magnetic flux. The 3D electromagnetic field simulations are also capable of determining the mutual inductance between current carrying elements.

This equivalent circuit is in theory accurate enough to model the response of the via up to a frequency approaching infinity. The problem with this circuit is that it is very complicated and takes a considerable amount of computation time to simulate. This makes it an unpractical model for use in a design process. The next equivalent circuit shown in figure 4 is a slightly more practicable model.

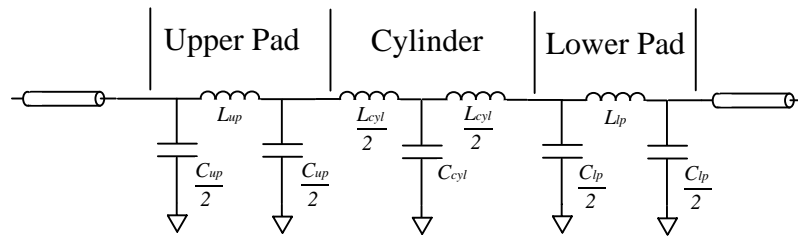


Figure 4. Via Equivalent Circuit (Distributed)

This circuit is referred to in this paper as the *distributed model*. Again this circuit uses a traditional lossless transmission line model. By using knowledge of the via's response this circuit can more accurately model the effect of the three segments of the via. The total response of the via at lower frequencies will tend to look capacitive, or low impedance. As frequencies increase, the effect of each segment will become more distinct. When this occurs, the first and third sections (the pads) will continue to look capacitive but the second section (the cylinder) will tend to look more inductive or higher impedance, as the cylinder diameter is reduced. The distributed equivalent circuit can portray this behavior more accurately. This circuit does not include any coupling elements so it cannot accurately model the via at as high of frequencies as the *coupled* circuit but still separates the via into three regions.

The last circuit, the *lumped circuit*, is the simplest model of the three equivalent circuits. It is shown in Figure 5.

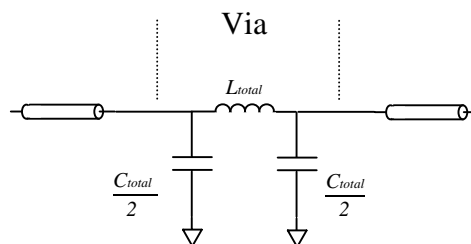


Figure 5. Via Equivalent Circuit (Lumped)

This circuit is very practical to be used in a development process due to its reduction in computation time in determining the response. The question is whether it can model the via's response to a high enough frequency. Figure 6 shows the transmitted response of all three equivalent circuits when an ideal step is introduced. Clearly the coupled equivalent circuit is capable of modeling much higher frequency components. What is of considerable interest is the step response when the bandwidth is limited to a more reasonable range. Figure 7 shows the transmitted response of the three equivalent circuits when a Gaussian step is incident. The Gaussian step shown is a 100ps rise-time, 10-pole Gaussian model that eliminates extremely high frequencies.

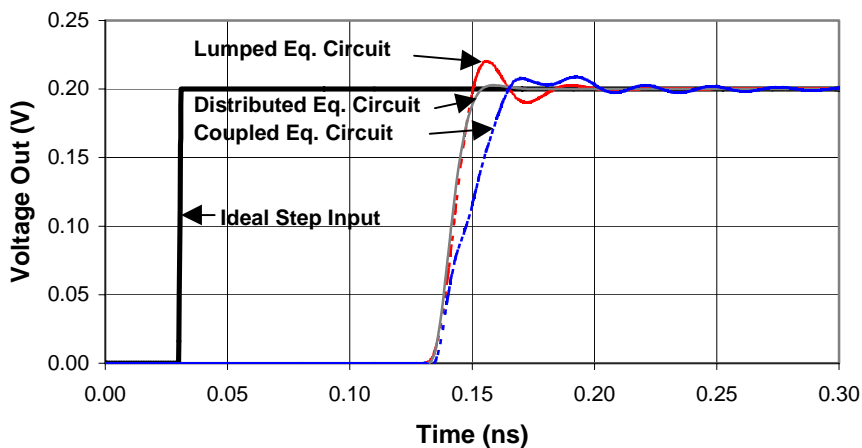


Figure 6. Ideal Step Response of the Via Equivalent Circuits

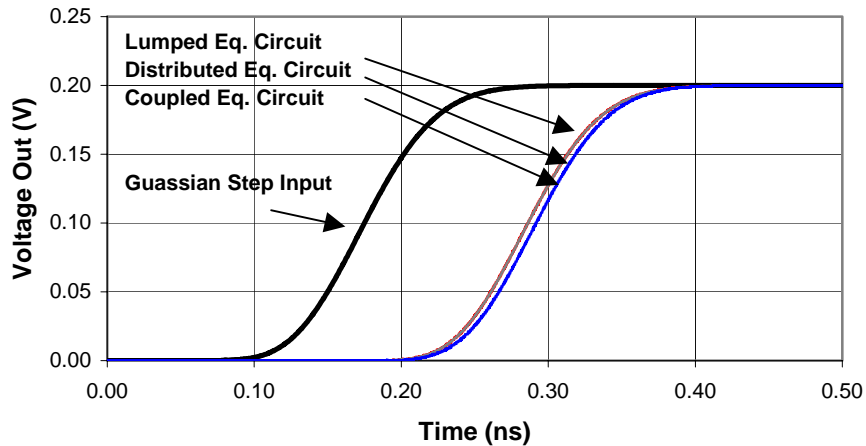


Figure 7. Gaussian Step Response of the Via Equivalent Circuits

This figure demonstrates that when the frequency is limited to the bandwidth of interest, all of the equivalent circuits tend to have a near identical response. Since this paper is interested in the response of signals with rise-times around the 100ps range, the *lumped* equivalent circuit will suffice for the rest of the analysis. Using this simplified circuit greatly reduces computation time in simulations while still accurately modeling the electrical response of the via.

Using the approximation that the *Rise-time Bandwidth Product* is equal to 0.35 ($t_r \cdot BW = 0.35$), a 100ps rise-time will correspond to a bandwidth of approximately 3.5 GHz. The TDR measurements use a 100ps rise-time step pulse. The Network Analyzer has a range of up to 6 GHz. The 100ps rise-time covers most signal rise-times seen today in high-speed digital circuits implemented on printed circuit boards.

The next chapter examines the results of the 3D electromagnetic field simulations.

CHAPTER V

3D ELECTROMAGNETIC FIELD SIMULATIONS

This chapter describes the results of simulations ran to extract the excess capacitance and inductance from the physical structure of a via. Figure 1 shows the geometric parameters that are swept during these simulations. The parameters are *pad radius*, *cylinder radius*, and *ground clearance radius*.

In the first set of simulations, the *pad radius* is swept to see the effect on capacitance and inductance. Figure 8 shows the effect that the *pad radius* has on capacitance. Three different sizes for *cylinder* and *ground clearance radius* are shown as the *pad radius* is swept. It can be seen that the capacitance increases as the pad radius increases. This is due to the fact that the surface area of the via is increasing and capacitance is proportional to the surface area of the conductors.

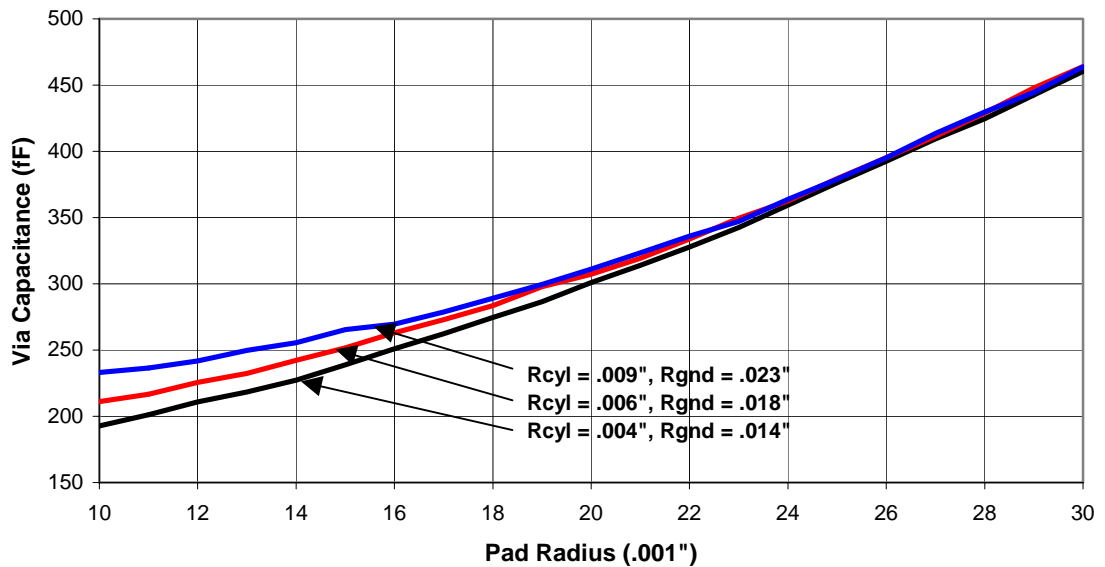


Figure 8. Via Capacitance Varying the Pad Radius

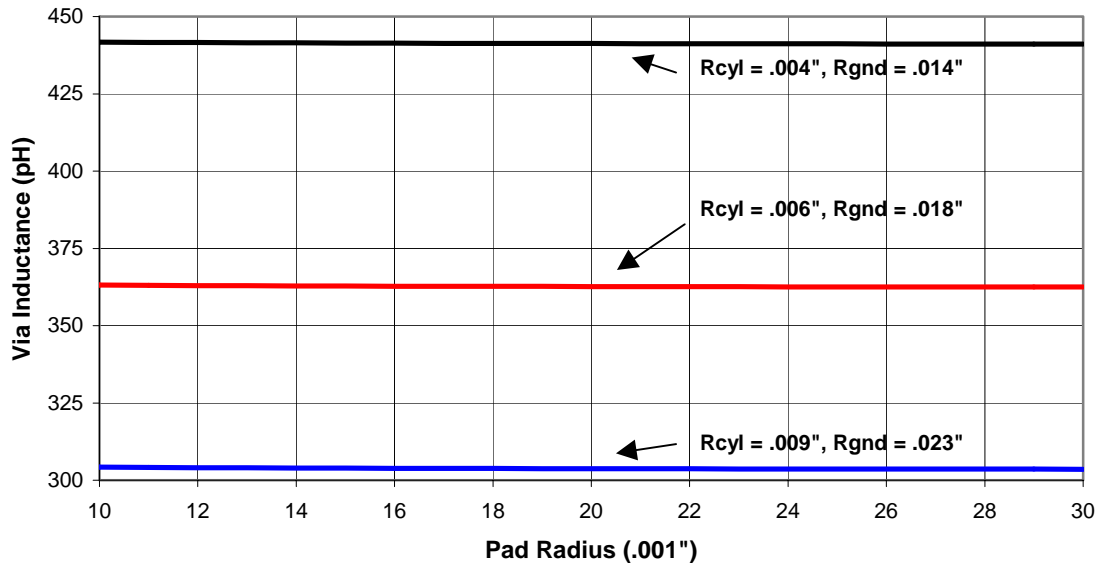


Figure 9. Via Inductance Varying the Pad Radius

Figure 9 shows the effect of pad radius on the via inductance for three sizes of cylinder and ground clearance radius. It can be seen that the inductance decreases slightly as the pad radius is increased. It is more obvious that the inductance is decreased as the cylinder radius is increased. This is due to the fact that the cross sectional area that the current flows through increases thus decreasing the resistance/inductance that the signal sees. Since the pad is only a small portion of the via that the current flows through compared to the cylinder, it is seen that the *cylinder radius* has the dominant effect on via inductance.

Using **Eq. 3** for the characteristic impedance of a lossless element, the effect of the *pad radius* on Z_0 can be graphed. Figure 10 shows this relationship. It is shown that Z_0 decreases as *pad radius* increases. This is mainly due to the capacitance increasing.

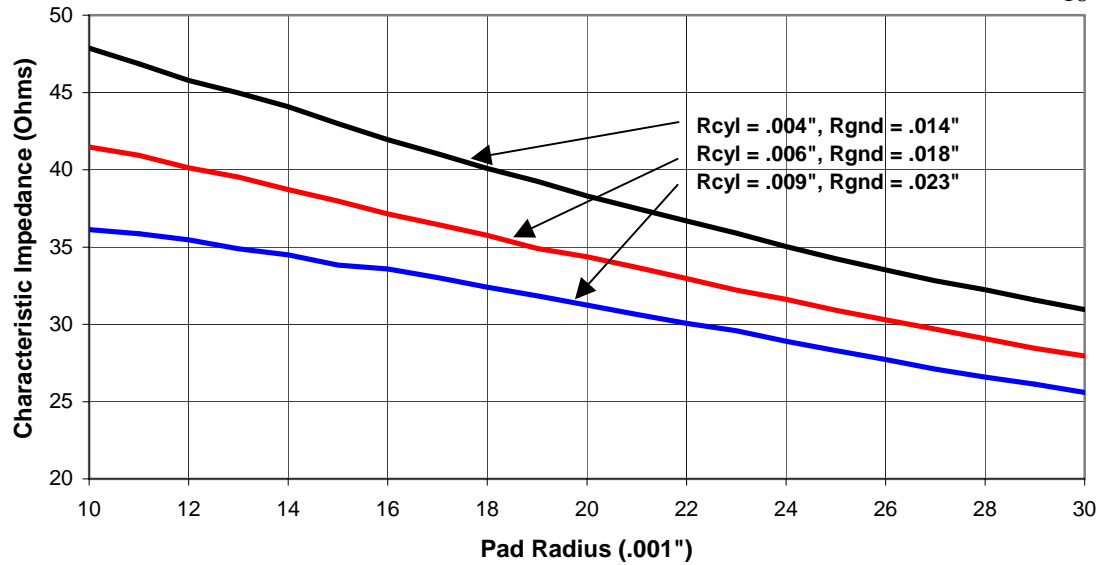


Figure 10. Zo Varying the Pad Radius

The next set of simulations were ran to examine the effect of *cylinder radius* on the capacitance and inductance of the via. Figure 11 shows the effect of *cylinder radius* on via capacitance. It is shown that the via capacitance increases as the *cylinder radius* is increased, again this is due to the surface area of the via increasing.

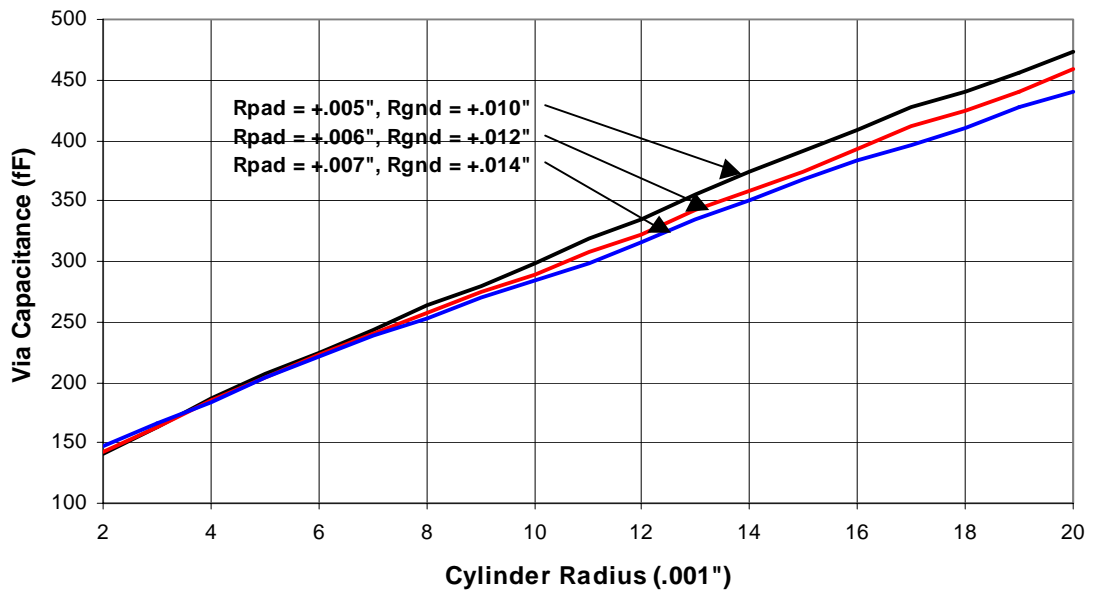


Figure 11. Via Capacitance Varying Cylinder Radius

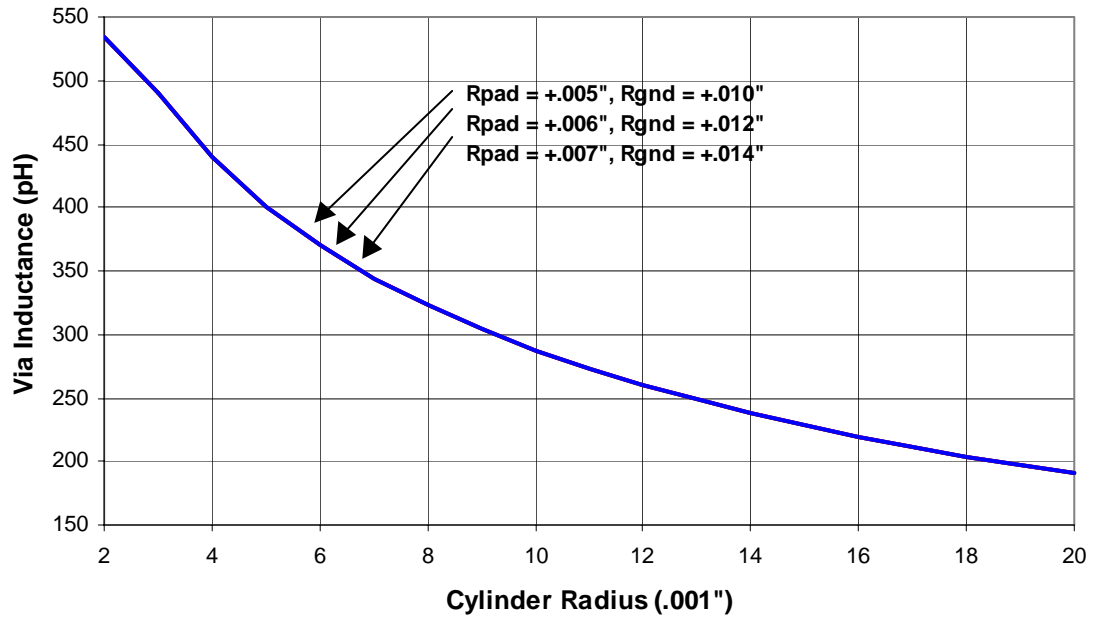


Figure 12. Via Inductance Varying Cylinder Radius

Figure 12 shows the effect that *cylinder radius* has on the via inductance. In this case, increasing the cylinder radius drastically reduces the inductance. Again this is due to increasing the cross-sectional area that the current has to flow through. It is also demonstrated that the *cylinder radius* is the dominant factor on inductance since the three plots of different pad and ground clearance radiuses are almost identical.

Figure 13 shows the characteristic impedance as a function of *cylinder radius*, again using **Eq. 3**. This shows that Z_o decreases as the *cylinder radius* increases. In this case, the decreasing Z_o is due to both an increasing capacitance and a decreasing inductance.

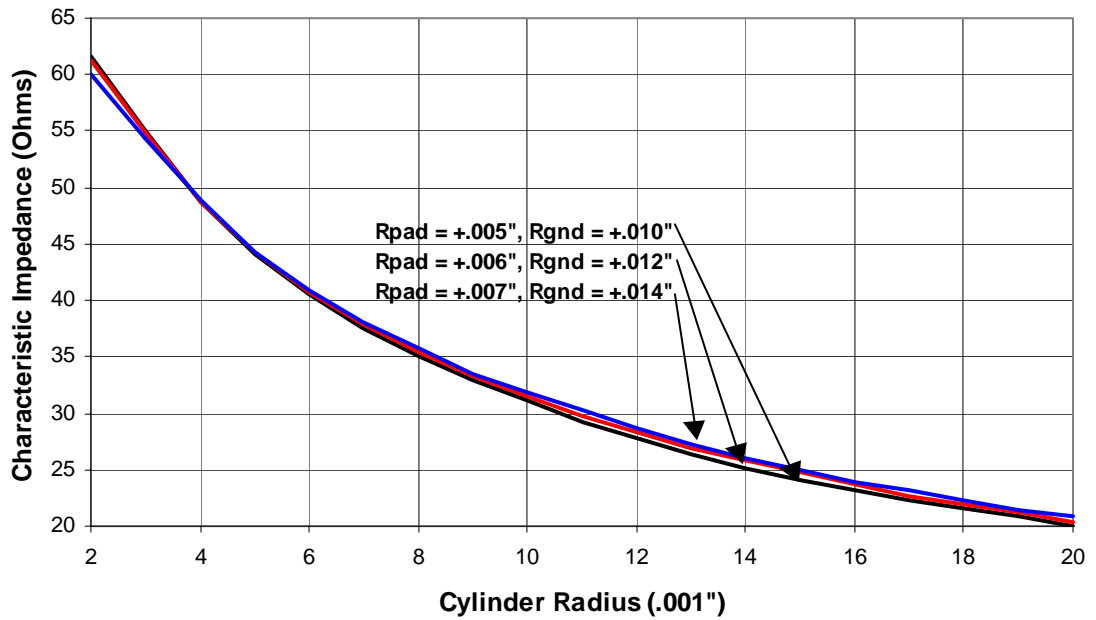


Figure 13. Zo Varying the Cylinder Radius

The next sets of simulations were ran considering the effect of *ground plane clearance radius*. Figure 14 shows the via capacitance as a function of *ground clearance radius*.

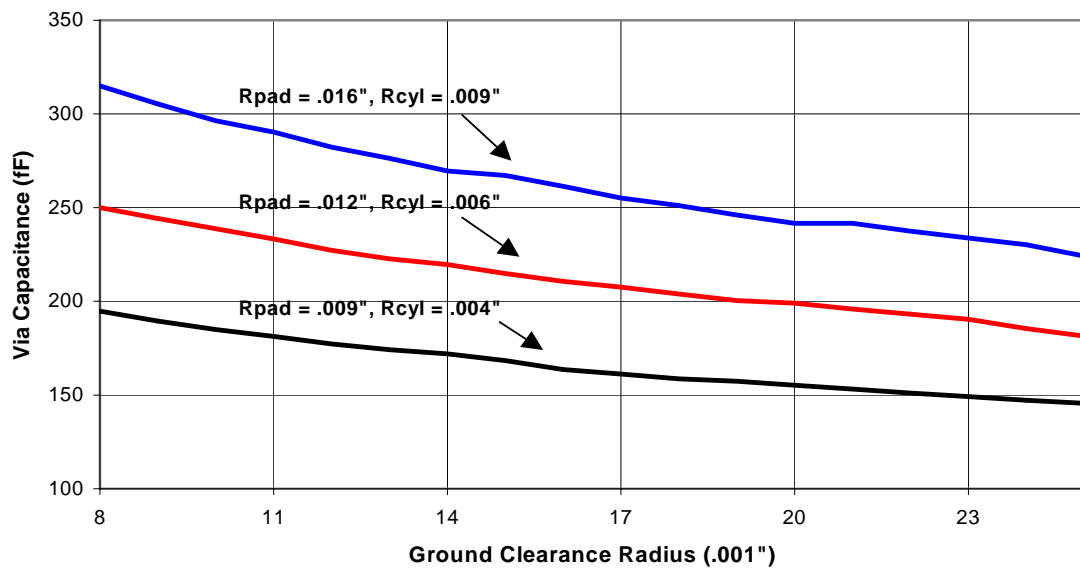


Figure 14. Via Capacitance Varying Ground Clearance Radius

It can be seen that as the distance between the ground plane and the via increases, the capacitance decreases. This is due to capacitance being inversely proportional to the distance between the two conducting plates of a capacitor.

Figure 15 shows the relationship between via inductance and *ground plane clearance radius*. The inductance decreases slightly even though it is difficult to see in figure 15. This is due to the magnetic field loop area between the ground plane and the conductor is decreasing as the ground plane is backed off.

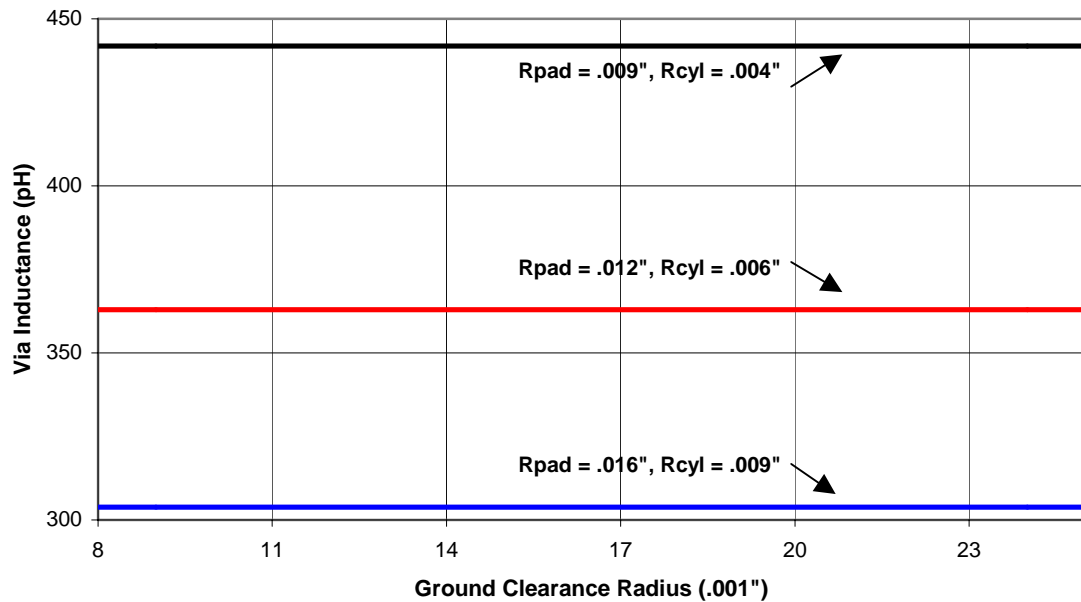


Figure 15. Via Inductance Varying Ground Clearance Radius

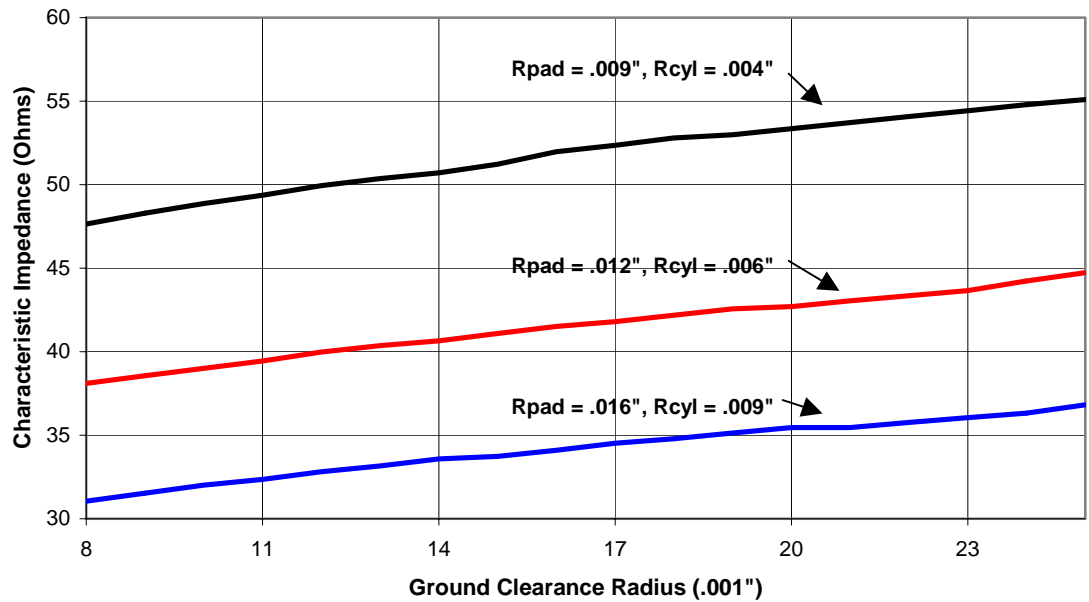


Figure 16. Z_o Varying Ground Clearance Radius

Figure 16 shows the characteristic impedance as a function of *ground plane clearance radius*. It is shown that Z_o increases as the clearance is increased. This is mainly due to the capacitance decreasing since the effect on inductance is minimal.

This chapter has examined the 3D EM field simulations that were ran to extract the inductance and capacitance from a physical model of a via. The next chapter looks at the time domain measurements taken on a test printed circuit board containing vias of various geometry's in order to verify that the simulation results track the empirical data.

CHAPTER VI

TIME DOMAIN ANALYSIS

This chapter examines the time domain measurements taken on a test printed circuit board containing vias of varying geometry's. This circuit board was designed to show the empirical effect of the via's physical geometry on its electrical effect. The time domain analysis is accomplished by using *Time Domain Reflectometry*, (TDR). Figure 17 shows the equivalent circuit of the TDR and test printed circuit board experimental setup. The TDR oscilloscope has an output impedance of 50Ω 's. In order to show the discontinuity caused by the via in more detail, the test printed circuit board uses 75Ω microstrip transmission lines. Since the TDR measurement gives the ability to separate discontinuities as a function of time, this mismatch does not effect the measurement. This equivalent circuit of the experimental setup shows the *lumped* equivalent circuit for the via.

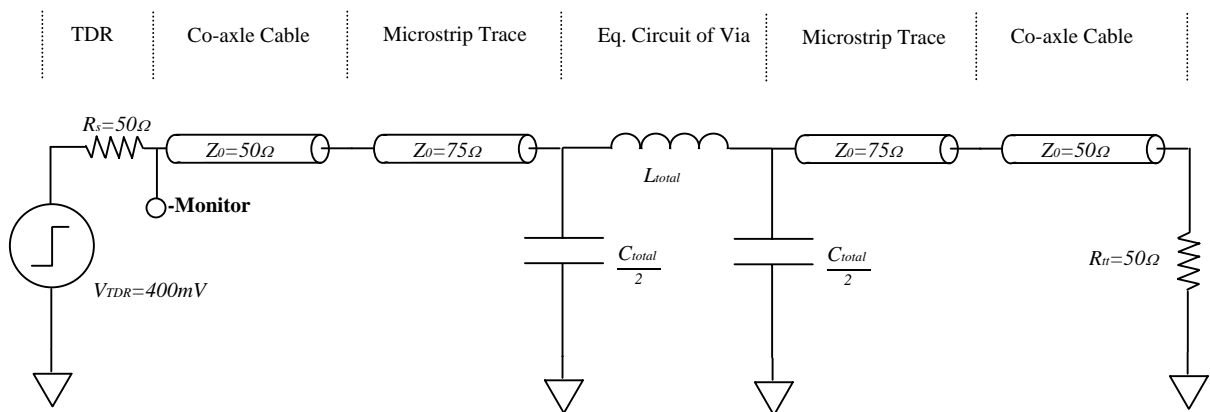


Figure 17. Equivalent Circuit of the Experimental Setup for TDR Measurements

Figure 18 shows the test printed circuit board developed to examine the empirical results of the electrical response of various via sizes. Figure 19 shows the laboratory setup used to take the TDR measurements.

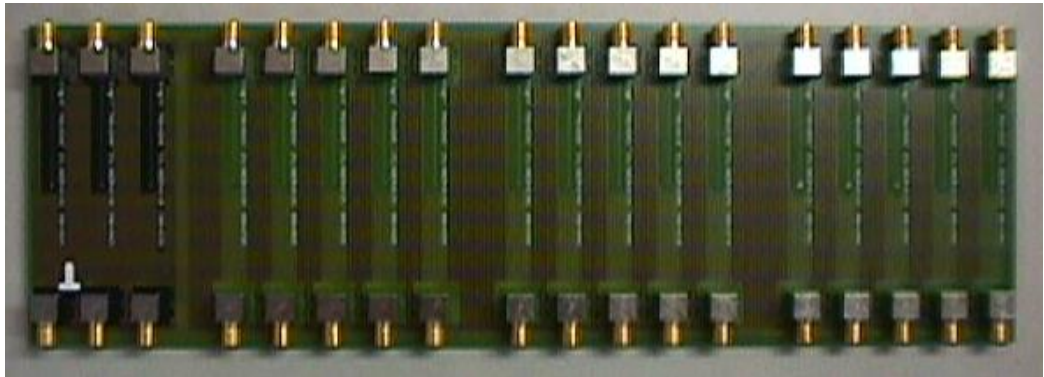


Figure 18. Test PCB Containing Various Via Geometry's

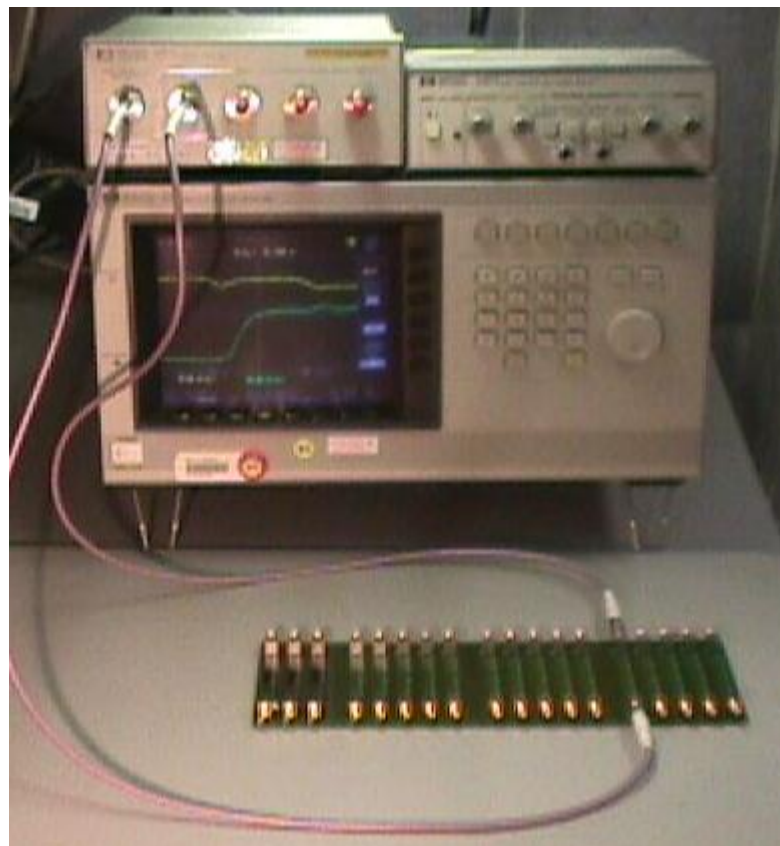


Figure 19. Laboratory Setup Used to Make TDR Measurements

The test printed circuit board has 15 vias that are used in this experiment. Five vias are used in each of the three parametric sweeps, *pad radius*, *cylinder radius*, and *ground clearance radius*. Figure 20 shows the first set of measurements varying *pad radius*. It can be seen that the impedance of the via decreases as the pad radius increases. This is consistent with the 3D EM Field simulations. The main factor contributing to this is the increase in capacitance due to the increase in surface area of the via. Clearly it is more desirable to have a smaller *pad*. The limit on the minimum size pad that can be used is often dictated by the printed circuit board manufacturer.

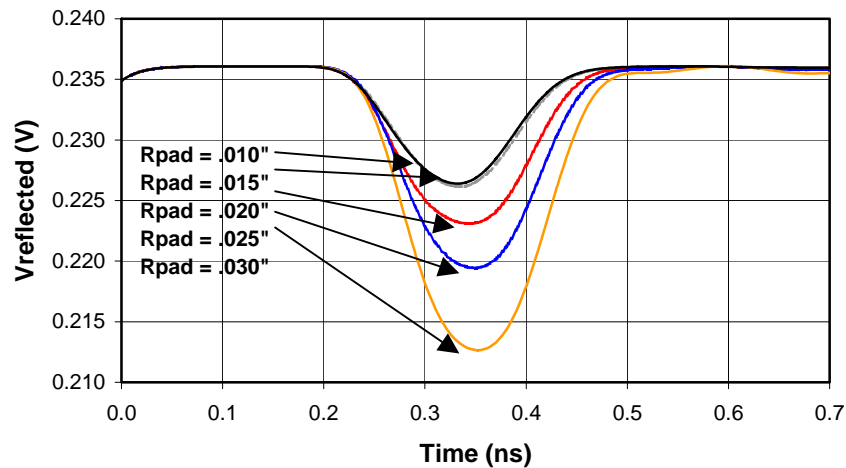


Figure 20. TDR Measurements of Microstrip Vias Varying the Pad Radius (Rcyl = .006", Rgnd = .018")

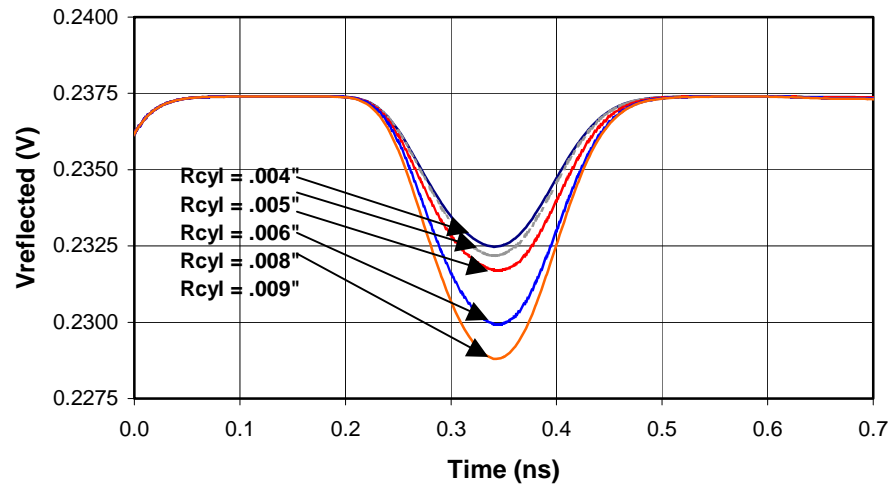


Figure 21. TDR Measurements of Microstrip Vias Varying the Cylinder Radius (Rpad = +.006\", Rgnd = +.012\")

Figure 21 shows the second set of measurements taken while varying the *cylinder radius*. Again it is shown that the impedance of the via decreases as the cylinder radius increases. This again verifies the results from the 3D EM Field simulations that show a decrease in inductance and an increase in capacitance as the cylinder radius is increased. It is clearly more desirable to have as small a cylinder radius as possible. This specification is limited by the minimum drill bit radius that the printed circuit board manufacturer has available.

Figure 22 shows the last set of measurements taken while varying the *ground plane clearance radius*. Here it is shown that the impedance increases as the ground plane radius increases. This again is consistent with the 3D EM Field simulations with the dominant factor being the decrease in capacitance.

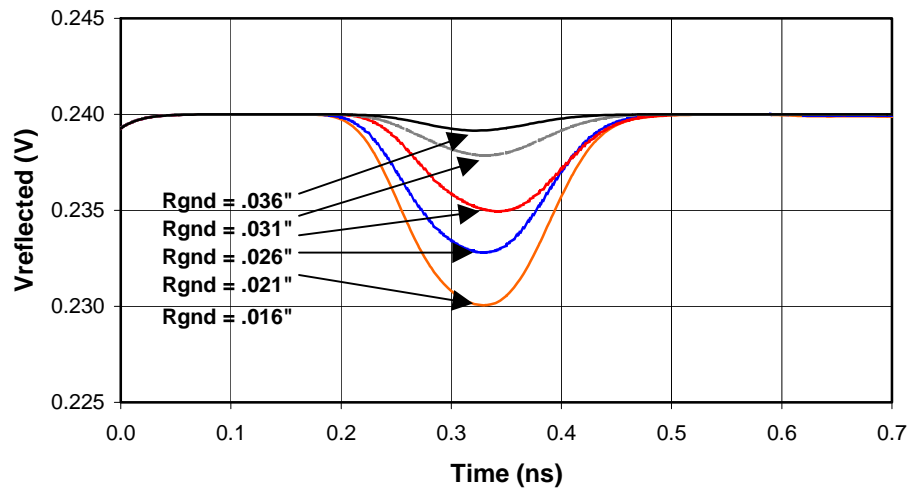


Figure 22. TDR Measurements of Microstrip Vias Varying the Ground Plane Clearance Radius ($R_{pad} = .012''$, $R_{cyl} = .006''$)

This chapter has illustrated that the equivalent circuit and 3D electromagnetic field simulations are capable of tracking the electrical response of empirical data in the time domain. The next chapter will investigate the accuracy of the via model in the frequency domain.

CHAPTER VII

FREQUENCY DOMAIN ANALYSIS

This chapter examines the frequency response of a via by taking Network Analyzer measurements on the test printed circuit board. This is accomplished by sweeping the input sinusoidal voltage and monitoring the reference, reflected, and transmitted voltages. The network analyzer allows these *S-parameters* to be extracted into a SPICE model so the equivalent circuit of the via can be compared to the empirical data in the frequency domain. Figure 23 shows the equivalent circuit of the Network Analyzer measurements made on the test printed circuit board. Figure 24 shows the laboratory setup of the Network Analyzer measurements.

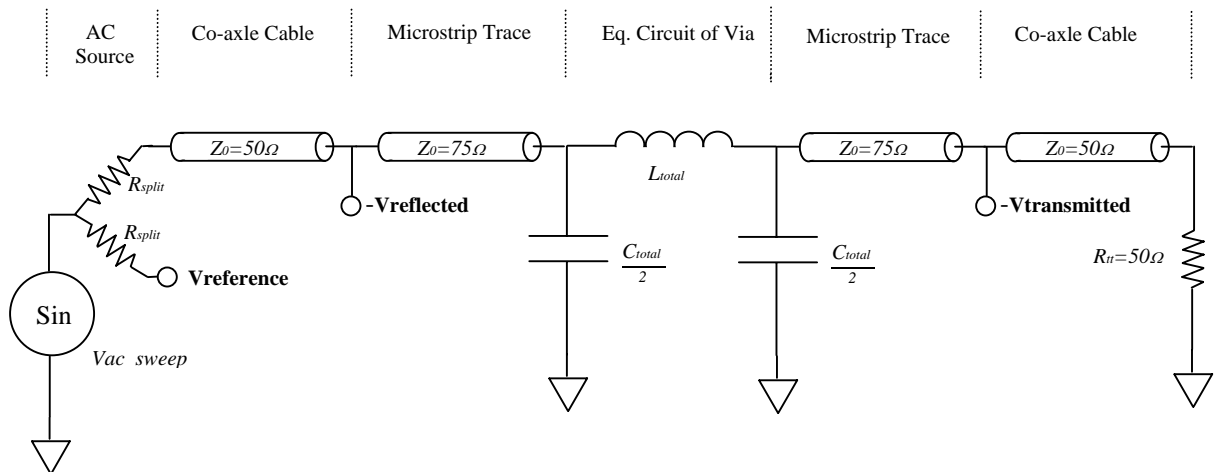


Figure 23. Experimental Setup of the Network Analyzer Measurements



Figure 24. Laboratory Setup Used to Make Network Analyzer Measurements

The frequency domain analysis was done on the same test printed circuit board as the time domain analysis. Figures 25 and 26 show the $|S_{11}|$ (reflected) and $|S_{21}|$ (transmitted) parameters of the test vias while varying *pad radius*.

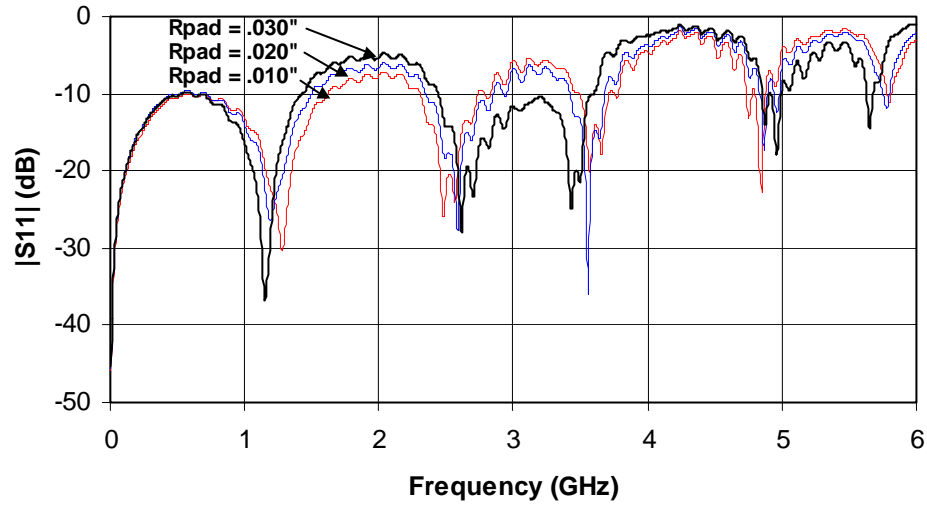


Figure 25. $|S_{11}|$ Measurements of Microstrip Vias Varying the Pad Radius ($R_{cyl} = .006''$, $R_{gnd} = .018''$)

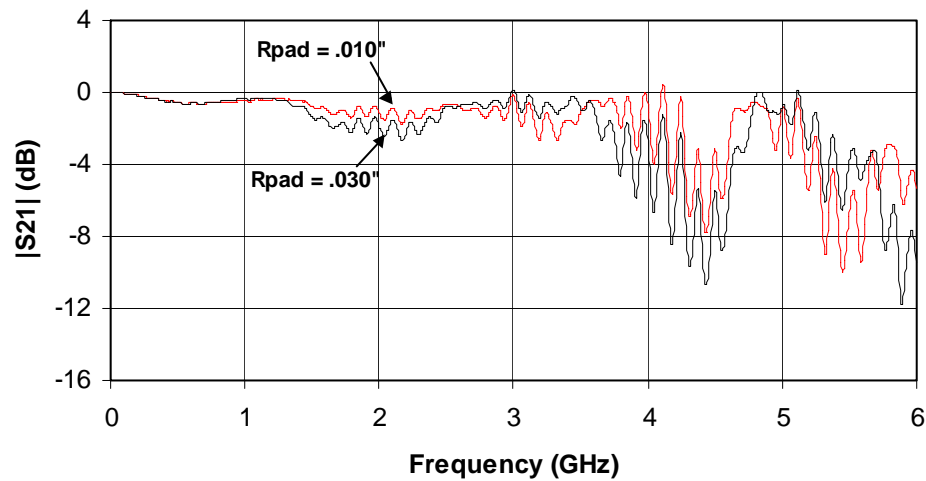


Figure 26. $|S_{21}|$ Measurements of Microstrip Vias Varying the Pad Radius ($R_{cyl} = .006''$, $R_{gnd} = .018''$)

Figures 27 and 28 show the $|S_{11}|$ and $|S_{21}|$ parameters of the of the test vias while varying *cylinder radius*.

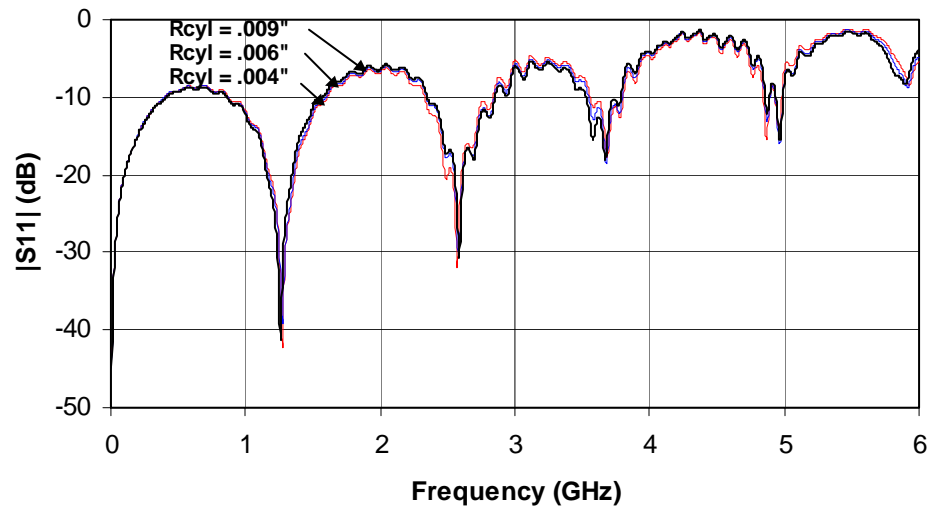


Figure 27. $|S_{11}|$ Measurements of Microstrip Vias Varying the Cylinder Radius ($R_{pad} = +.006''$, $R_{gnd} = +.012''$)

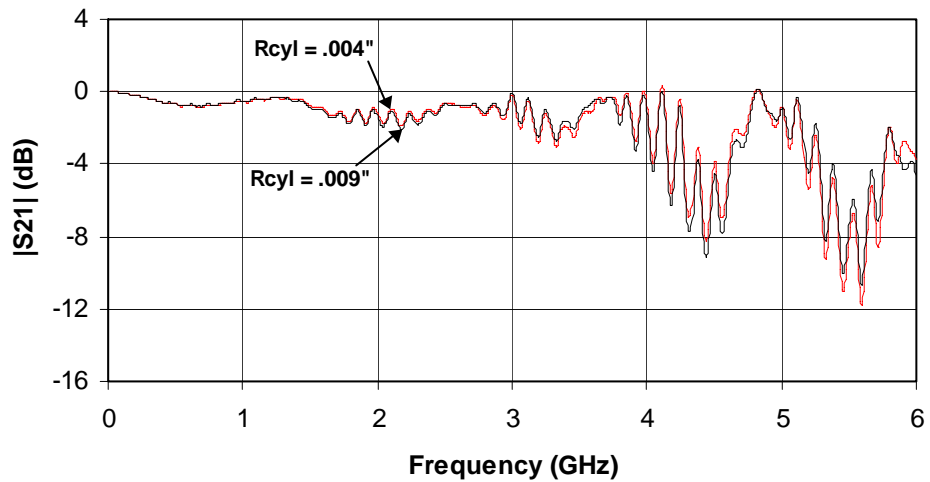


Figure 28. $|S_{21}|$ Measurements of Microstrip Vias Varying the Cylinder Radius ($R_{pad} = +.006''$, $R_{gnd} = +.012''$)

Figures 29 and 30 show the $|S_{11}|$ and $|S_{21}|$ parameters of the of the test vias while varying *ground clearance radius*.

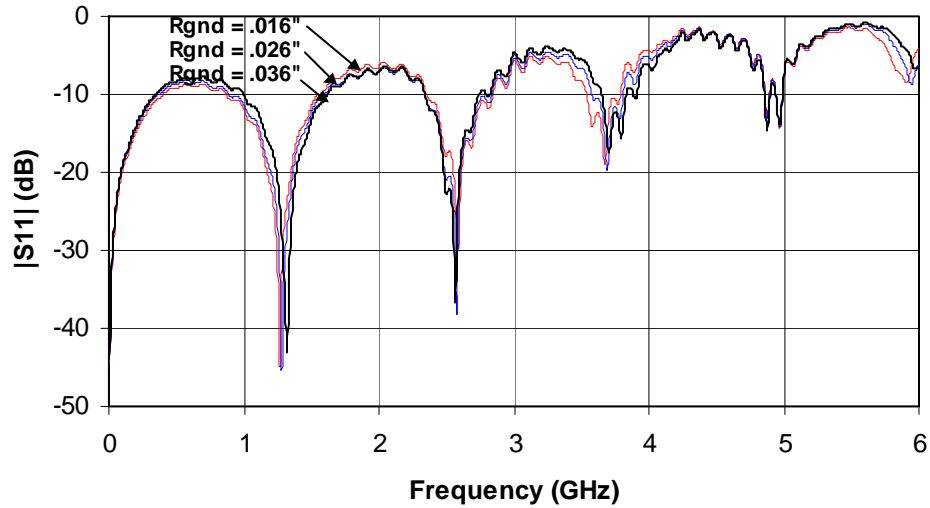


Figure 29. $|S_{11}|$ Measurements of Microstrip Vias Varying the Ground Clearance Radius ($R_{pad} = .012''$, $R_{cyl} = .006''$)

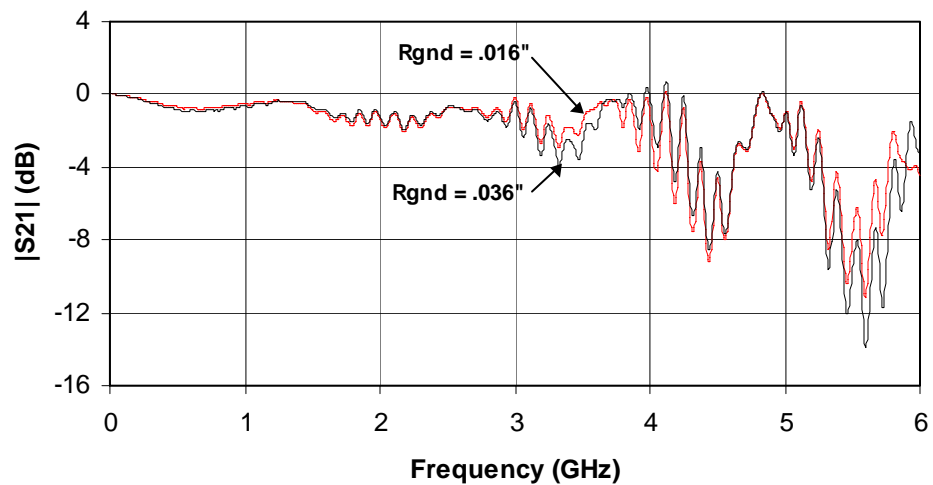


Figure 30. $|S_{21}|$ Measurements of Microstrip Vias Varying the Ground Clearance Radius ($R_{pad} = .012''$, $R_{cyl} = .006''$)

The frequency response of the via is contained within the scattering parameter data displayed in these figures. The difficulty in analyzing it is in the separation of the via's response to the response of all the other elements in the system. In the time

domain measurements made in the previous chapter, the effect of the via could be separated into a discrete range of time. This allowed the response of the PCB connectors and trace to be ignored by zooming in on only the region in time where the via's response was apparent. Unfortunately in the frequency domain, this is not possible. The capacitive and inductive effect of the via is present at all frequencies so it cannot be isolated. The $|S_{11}|$ and $|S_{21}|$ data shown in figures 25-30 includes the frequency response of the connectors and the trace in addition to the response of the via. This makes it very difficult to examine what effect the via has on this data. In all three sets of measurements (*Rpad*, *Rcyl*, and *Rgnd*), the scattering parameter data does not seem to change much as the geometric size of the via is swept. This indicates that the frequency response of the system is dominated by the other elements in the system besides the via.

The main conclusion that can be drawn from these Network Analyzer measurements is that when the element of interest is not easily isolated, a *Time Domain Reflectometry* measurement is probably the best choice for analysis.

CHAPTER VIII

CONCLUSION

This paper had presented an equivalent circuit for the characterization of a printed circuit board via. It was demonstrated in Chapter 4 that the *lumped* equivalent circuit was sufficient to model the electrical response for signal rise-times on the order of 100ps. 3D electromagnetic field simulations were then ran to extract the electrical parameters C and L for various sizes of via structures. Time Domain measurements were taken on a test printed circuit board to verify the accuracy of the equivalent circuit using the 3D EM simulation results. Three sets of test vias were examined. One via from each set of TDR measurements is compared to the corresponding SPICE simulation results of the experimental setup in figures 31-33.

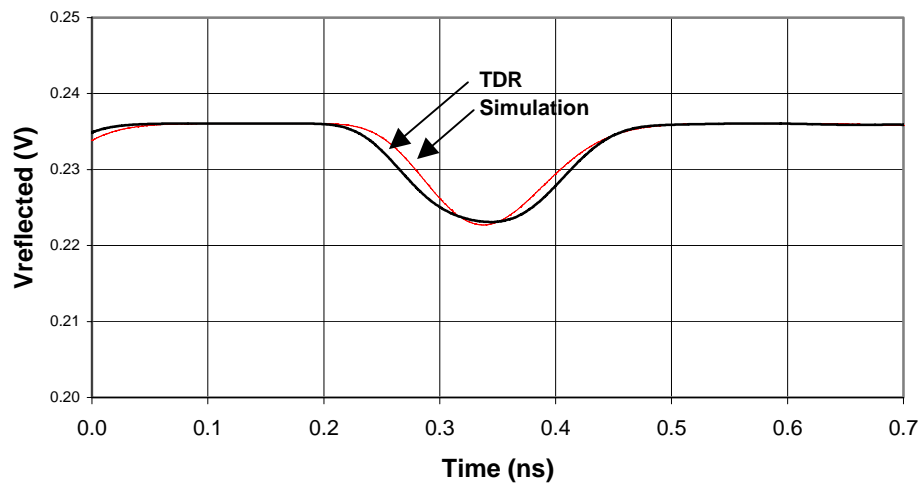


Figure 31. Comparison of TDR Measurements with Simulation Results (Pad Radius Example)

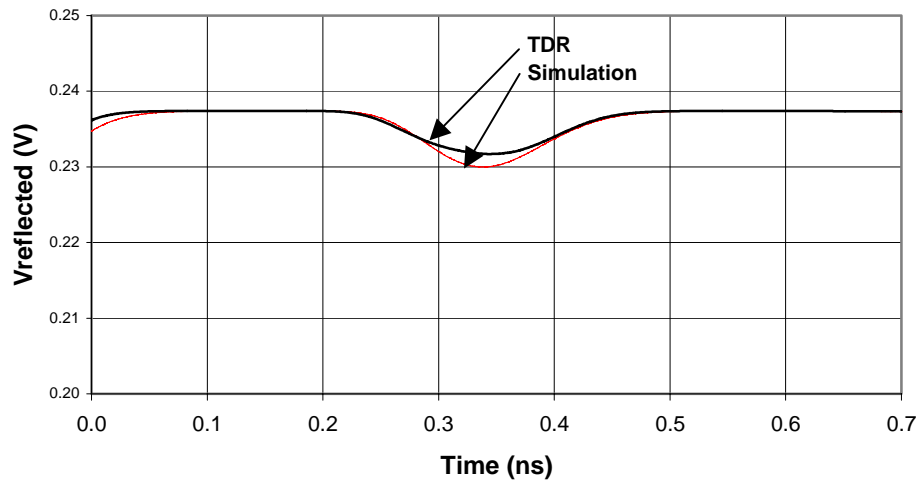


Figure 32. Comparison of TDR Measurements with Simulation Results (Cylinder Radius Example)

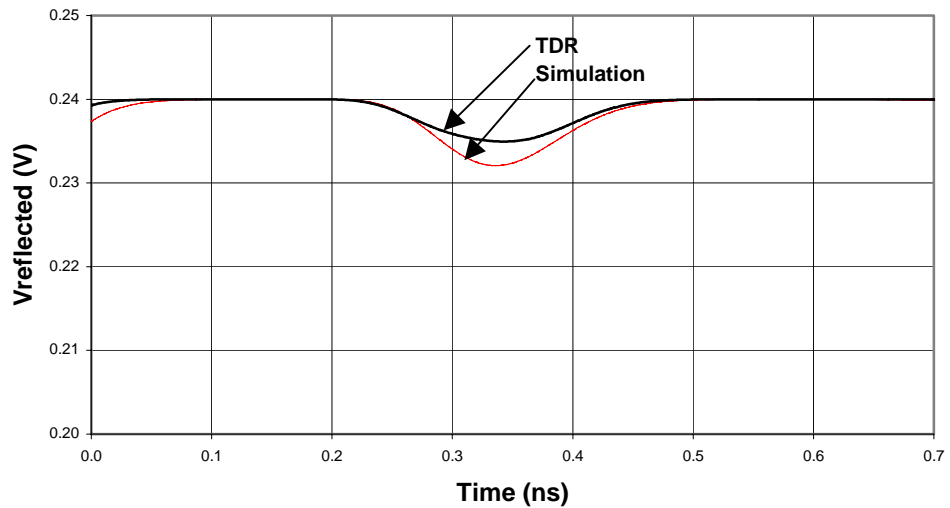
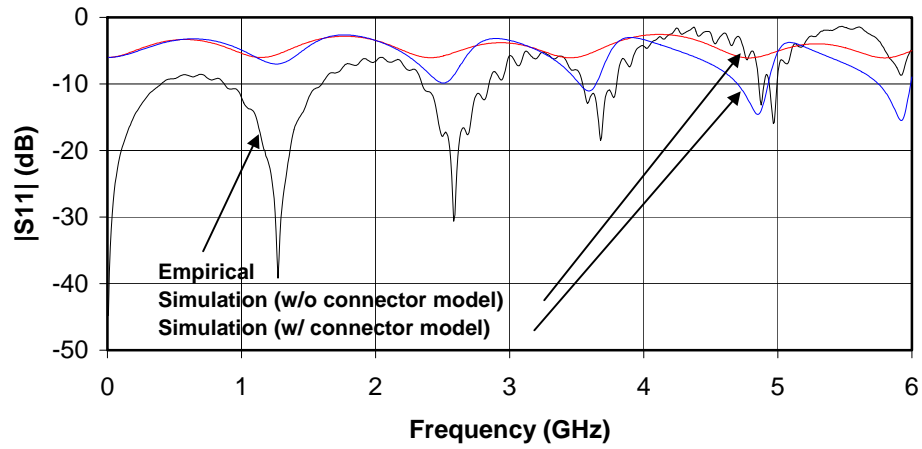


Figure 33. Comparison of TDR Measurements with Simulation Results (Ground Clearance Radius Example)

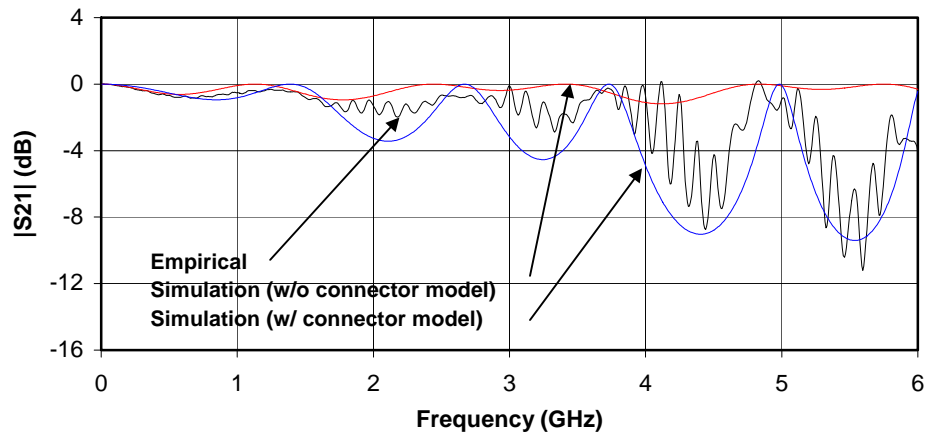
These comparisons verify that the equivalent circuit is an accurate representation of the electrical response of a microstrip via for the bandwidth under consideration. They also illustrate that the 3D electromagnetic field simulations are able to extract electrical parameters that when used in the equivalent circuit presented accurately model the empirical response of the via in the time domain.

Chapter 7 presented the Network Analyzer measurements taken on the test printed circuit board. It was discussed that the actual response of the via is *hidden* in the *S-parameter* measurements taken due to the difficulty in isolating the via from the rest of the *Device Under Test*. A frequency domain analysis on the equivalent circuit was done in SPICE to verify its accuracy in the frequency domain. The equivalent circuit of just the via and microstrip traces connecting to it did not match the empirical results very accurately. A second simulation was ran including an L (1pH) and C (1pF) for each of the two PCB connectors that are present on the board. This simulation matched the Network Analyzer measurements more closely. It should be noted that the response of the via is not the most dominant factor in these measurements.

Figures 34 and 35 show the $|S_{11}|$ and $|S_{21}|$ measurements taken of the test printed circuit board compared to the equivalent circuit simulations ran in SPICE. Both the simulations with and without the model of the PCB connectors are shown.



**Figure 34. Comparison of $|S_{11}|$ Measurements to Simulation Results
($R_{pad} = .012''$, $R_{cyl} = .006''$, $R_{gnd} = .018''$)**



**Figure 35. Comparison of $|S_{21}|$ Measurements to Simulation Results
($R_{pad} = .012''$, $R_{cyl} = .006''$, $R_{gnd} = .018''$)**

To illustrate the effect that the via has on the frequency domain measurements, a simulation was ran comparing the equivalent circuit of the via (including the PCB connectors and trace) to a simulation of the PCB without a via present. The equivalent circuit of the later simulation consists of only the PCB connectors and trace. Figures 36 and 37 show the *S-parameter* SPICE simulation comparison of the two cases.

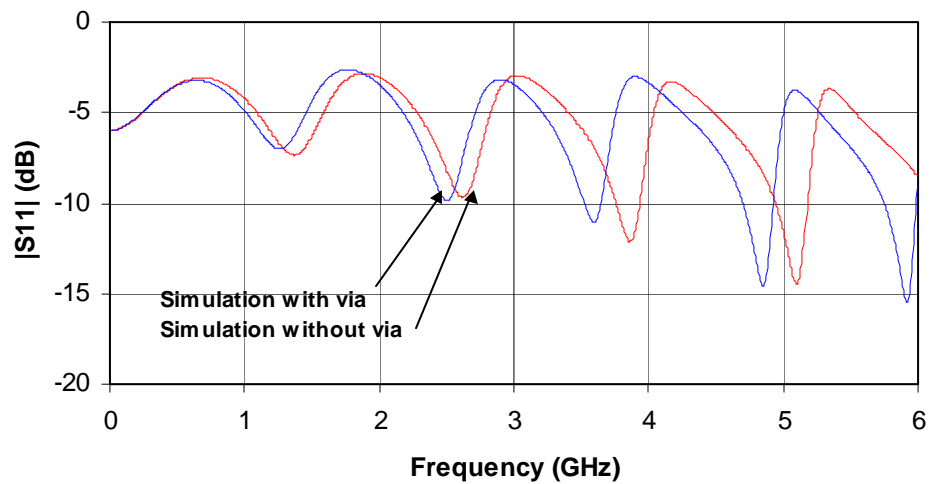


Figure 36. Comparison of $|S_{11}|$ Simulations with and without the Via Equivalent Circuit

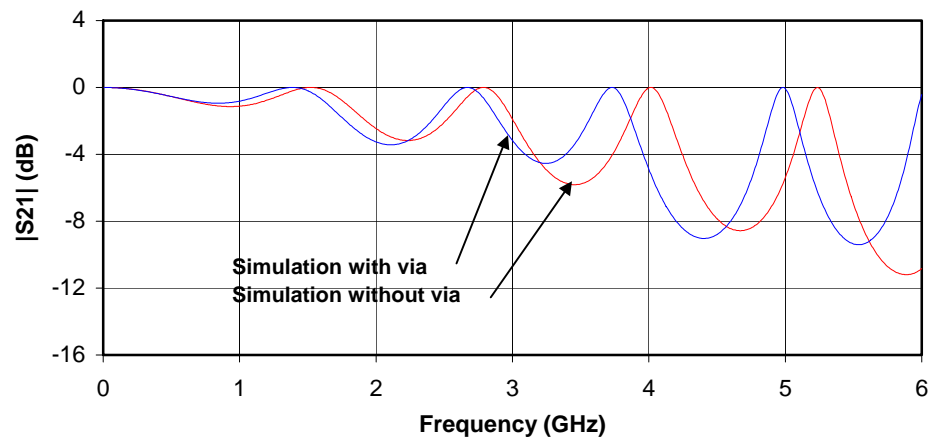


Figure 37. Comparison of $|S_{21}|$ Simulations with and without the Via Equivalent Circuit

These figures show that the presence of the via causes the nulls and valleys of the frequency response to shift to higher frequencies.

This paper has demonstrated through simulation and empirical measurements that the *lumped* equivalent circuit presented in Chapter 4 can accurately model a microstrip via's electrical response. It has also illustrated that when used in conjunction with a 3D Electromagnetic field simulator, the electrical parameters for the equivalent circuit can be found.

The next section gives a list of *design guidelines* drawn from the results of this investigation when using vias to connect microstrip transmission lines on a printed circuit board.

Design Guidelines

- [1] **Use the minimum size drill bit for creating the via cylinder. This has less to do with lowering the capacitance of the via and more to do with raising its inductance. Since a via looks like a region of low impedance compared to a traditional printed circuit board transmission line, raising the inductance will increase its characteristic impedance to better match the connecting lines.**
- [2] **Use the minimum size pad that the PCB manufacturer allows. The pad is the source of the most capacitance. The ideal case would be to connect the transmission lines directly to the via cylinder.**
- [3] **Do not use the minimum size ground clearance radius. This is counter-intuitive since in most cases, smaller is better. By having a small portion of the connecting traces near the via NOT run over a ground plane, two regions of higher impedance immediately before and after the via are introduced. These regions of higher impedance will counter the lower impedance characteristic of the via and better match the line. This effect can also be accomplished by placing very small surface mount inductors in series with the via immediately before and after.**
- [4] **Use the thinnest printed circuit board possible. This will reduce the overall height of all vias on the board. Reducing the height of the via will decrease the length of the discontinuity that the signal has to pass through.**
- [5] **Place vias that connect the ground planes together near the signal vias that pass through multiple ground planes. This provides a low impedance path for the return current to flow when the signal changes layers. This will reduce the discontinuities caused by the via.**

When designing high-speed transport systems implemented on printed circuit boards, signal integrity is of great importance. Discontinuities can lead to reflections, signal rise-time degradation, and may cause unexpected switching in digital systems. A common source of discontinuity in multi-layered printed circuit boards is when a transmission line changes signal layers using a *via*. When designing a high-speed

system, all sources of discontinuities must be modeled in order to account for their negative effects. By accurately modeling the printed circuit board via and knowing what physical dimensions effect its electrical response a designer can counter its parasitic effects. This paper has presented an accurate model for the printed circuit board via that can be used in a development process. By using this model in conjunction with 3D electromagnetic simulations, the negative effect of the printed circuit board via can be avoided.

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\$\$\$----- Parameter Definition -----\$\$\$

PARAM

```

Pad_R      = 29
Pad_H      = 1.1
Pad_Above  = 20
Gnd_Backoff = 30
Gnd_H      = 2.2
Gnd_W      = 10000
Gnd_L      = 10000
Diel_Const = 4.3
window_x   = 10000
window_y   = 10000
window_z   = 10000
VAR_SET_GRID = 100000;
VAR_ITER_TOL = 1e-15;

```

\$\$\$----- (Ground Plane) -----\$\$\$

BLOCK

```

NAME      = Ground_Plane;
V1        = 0, -(Gnd_H/2), 0;
DIRECTION = 0, 1, 0;
WIDTH     = Gnd_W;
LENGTH    = Gnd_L;
HEIGHT    = Gnd_H;
VOLT      = 0;

```

CYLINDER

```

NAME      = Diel_Spacer;
V1        = 0, (-Gnd_H/2), 0;
DIRECTION = 0, 1, 0;
HEIGHT    = Gnd_H;
RADIUS    = Gnd_Backoff;
DIEL      = Diel_Const;

```

\$\$\$----- (Dielectric Spacing) -----\$\$\$

BLOCK

```

NAME      = Diel_Spacer;
V1        = 0, (Gnd_H/2), 0;
DIRECTION = 0, 1, 0;
WIDTH     = Gnd_W;
LENGTH    = Gnd_L;
HEIGHT    = Pad_Above - Gnd_H/2;
DIEL      = Diel_Const;

```

BLOCK

```

NAME      = Diel_Spacer;
V1        = 0, -(Gnd_H/2), 0;
DIRECTION = 0, -1, 0;
WIDTH     = Gnd_W;
LENGTH    = Gnd_L;
HEIGHT    = Pad_Above - Gnd_H/2;
DIEL      = Diel_Const;

```

\$\$\$----- (Upper Via Pad) -----\$\$\$

CYLINDER

```

NAME      = Upper_Via_Pad;
V1        = 0, (Pad_Above), 0;
DIRECTION = 0, 1, 0;
HEIGHT    = Pad_H;
RADIUS    = Pad_R;
VOLT      = 1;

```

```
$$$----- (Via Cylinder)-----$$$
```

```
CYLINDER
```

```
  NAME      = Via_Cylinder;
  V1        = 0, (-Pad_Above), 0;
  DIRECTION = 0, 1, 0;
  HEIGHT    = 2*Pad_H;
  RADIUS    = Cyl_R;
  VOLT      = 1;
```

```
$$$----- (Lower Via Pad)-----$$$
```

```
CYLINDER
```

```
  NAME      = Lower_Via_Pad;
  V1        = 0, -(Pad_Above), 0;
  DIRECTION = 0, -1, 0;
  HEIGHT    = Pad_H;
  RADIUS    = Pad_R;
  VOLT      = 1;
  COLOR     = Pad_C;
```

```
$$$----- (Simulation Window)-----$$$
```

```
WINDOW3D
```

```
  V1          = -window_x, -window_y, -window_z;
  V2          = window_x, window_y, window_z;
```

```
$$$----- (Set Options)-----$$$
```

```
OPTIONS
```

```
  UNIT      = 2.54e-5;
  SET_GRID  = VAR_SET_GRID;
  ITER_TOL  = VAR_ITER_TOL;
```

```
$$$----- (Calculations)-----$$$
```

```
CAPACITANCE
```

```
$$$-- END-----$$$
```

ii. Inductance

```

* RI3   RUN OUTPUT=Lvia_RI3.out
-----$
$--    Characterization of a Printed Circuit Board Via    --$
$--
$--    Purpose:      Inductance of a Printed Circuit Board Via  --$
$--
$--    Student:     Brock J. LaMeres                          --$
$--                University of Colorado                    --$
$--                Electrical and Computer Engineering Department --$
$--
$--    Begin Date:  August 1999                               --$
$--    End Date:   May    2000                               --$
$--
$--    Purpose:     This file describes the three dimensional  --$
$--                geometry of a printed circuit board via passing --$
$--                through one ground plane.  The goal is to find --$
$--                the inductance of the via with respect to the  --$
$--                ground plane.                               --$
$--
$--                Structures defined later in the file will  --$
$--                overlap the earlier structures.  This allows --$
$--                hollow conductors to be made.              --$
$--
$--    Units:       Set so that 1 = 1 mil (2.54e-5 meters)    --$
$--
$--    Variables:   -----  <- Pad                          --$
$--                |      <- Cylinder                        --$
$--                -----  <- Ground Plane Backoff          --$
$--                -----
$--
$--    Pad_R       :  Radius of the Via Pad                    --$
$--    Pad_H       :  Thickness Via Pad                        --$
$--    Cyl_R       :  Radius of the Via Cylinder               --$
$--    Pad_Above   :  Distance above the Ground Plane         --$
$--    Gnd_Backoff :  Ground Plane Clearance                  --$
$--    Gnd_H       :  Ground Plane Thickness                  --$
$--    Gnd_W       :  Width of Ground Plane                   --$
$--    Gnd_L       :  Length of Ground Plane                  --$
$--    Gnd_C       :  Color of Ground Plane                   --$
$--    window_x    :  X Coordinate of Simulation Window      --$
$--    window_y    :  Y Coordinate of Simulation Window      --$
$--    window_z    :  Z Coordinate of Simulation Window      --$
$--
$-----$

```

\$\$\$----- Parameter Definition -----\$\$\$

```
PARAM
  Pad_R      = 20
  Pad_H      = 1.1
  Cyl_R      = 1.1
  Pad_Above  = 15
  Gnd_Backoff = 30
  Gnd_H      = 2.2
  Gnd_W      = 10000
  Gnd_L      = 10000
```

\$\$\$----- Node Definition -----\$\$\$

\$\$\$--- Ground Plane ---\$\$\$

```
PLANE NODE
  NAME=Ground;
  NORMAL=0,1,0;
  CENTER=0,0,0;
  L1=Gnd_W;
  L2=Gnd_L;
  N1=4;
  N2=4;
```

```
NODE
  NAME=Backoff_Top;
  POSITION=0, Gnd_H/2, 0;
```

```
NODE
  NAME=Backoff_Bottom;
  POSITION=0, -Gnd_H/2, 0;
```

\$\$\$--- Upper Pad Top ---\$\$\$

```
NODE
  NAME=Upper_Pad_Top
  POSITION=0, (Pad_Above + Pad_H), 0;
```

\$\$\$--- Upper Pad Bottom ---\$\$\$

```
NODE
  NAME=Upper_Pad_Bottom;
  POSITION=0, Pad_Above, 0;
```

\$\$\$--- Cylinder Top ---\$\$\$

```
NODE
  NAME=Cylinder_Top
  POSITION=0, (-Pad_Above), 0;
```

\$\$\$--- Cylinder Bottom ---\$\$\$

```
NODE
  NAME=Cylinder_Bottom
  POSITION=0, (Pad_Above), 0;
```

\$\$\$--- Lower Pad Top ---\$\$\$

```
NODE
  NAME=Lower_Pad_Top
  POSITION=0, (-Pad_Above), 0;
```

\$\$\$--- Lower Pad Bottom ---\$\$\$

```
NODE
  NAME=Lower_Pad_Bottom;
  POSITION=0, -(Pad_Above + Pad_H), 0;
```


\$\$\$----- Current Element Definition -----\$\$\$

PLANE

NAME=Ground_Plane;
 BASE_NODE=Ground;
 H=Gnd_H;
 RHO=0;

SINGLE_BAR

NAME=Gnd_Backoff;
 NODE1=Backoff_Top;
 NODE2=Backoff_Bottom;
 W=1.772*Gnd_Backoff;
 H=1.772*Gnd_Backoff;
 RHO=1000000000000;

\$\$\$-- Upper Pad ---\$\$\$

SINGLE_BAR

NAME=Upper_Pad;
 NODE1=Upper_Pad_Top;
 NODE2=Upper_Pad_Bottom;
 W=1.772*Pad_R;
 H=1.772*Pad_R;
 RHO=0;

\$\$\$-- Cylinder ---\$\$\$

SINGLE_BAR

NAME=Cylinder;
 NODE1=Cylinder_Top;
 NODE2=Cylinder_Bottom;
 W=1.772*Cyl_R;
 H=1.772*Cyl_R;
 RHO=0;

\$\$\$-- Lower Pad ---\$\$\$

SINGLE_BAR

NAME=Lower_Pad;
 NODE1=Lower_Pad_Top;
 NODE2=Lower_Pad_Bottom;
 W=1.772*Pad_R;
 H=1.772*Pad_R;
 RHO=0;

\$\$\$----- Simulation Options -----\$\$\$

OPTIONS3I UNIT=2.54e-5;

\$\$\$--- Merging Ground Plane Hole ---\$\$\$

MERGE3I Upper_Pad_Bottom Ground000_000
 MERGE3I Cylinder_Bottom Ground000_000
 MERGE3I Lower_Pad_Bottom Ground000_000

\$\$\$----- Post-Processing Commands -----\$\$\$

\$- Define Signal Node

EXT Upper_Pad_Top
 EXT Cylinder_Top
 EXT Lower_Pad_Top

\$- Define Reference (Ground) Node

REF Ground000_000

\$- Calculation

FREQUENCY START_FREQ=20e9; END_FREQ=20e9; DECADE=1;

[B] SPICE Simulation Files

i. Transient Analysis

```
*****
* Name:          Time Domain Analysis of PCB Via          *
*                                                       *
* Student:       Brock J. LaMeres                        *
*               University of Colorado                   *
*               Electrical and Computer Engineering Department *
*                                                       *
* Begin Date:    August 1999                             *
* End Date:      July   2000                             *
*                                                       *
* Purpose:       This SPICE deck models the time domain reflectometry *
*               analysis of the pcb via equivalent circuit. *
*               The empirical data measured using a TDR oscilloscope *
*               is also displayed.                       *
*                                                       *
*****

*** Simulation Options *****
.OPTION Map
.TRANS 1p 4n

*** This is the test circuit to look at simulation results *****

.PARAM Clumped = 199f
.PARAM Llumped = 363p

XStepGen2  %Vtdr_Lumped 'StepGen'   (30p 125p .2 0 50 )

Tlump1  %Vtdr_Lumped %0 %999 %0  Z0=50 td=906p
Tlump2  %999 %0 %998 %0  Z0=75 td=200p

Clump1  %998 %0 VALUE=Clumped/2
Llump1  %998 %997 VALUE=Llumped
Clump2  %997 %0 VALUE=Clumped/2

Tlump3  %997 %0 %Vlump_out %0  Z0=75 td=260p
Rterm   %Vlump_out %0 50

*** This is the circuit for looking at TDR Results *****

Vtdr  %V_file %0  TRAN=PWL(
.INCLUDE "Via_8_TDR_100psModeled.tdr")
Rfile  %V_file %0  VALUE=50
```

```

*****
*** SUBCIRCUIT
*****

.SUBCKT 'StepGen'
+ %Out
+ (td tr VHi VLo Zo)
.PARAM V Hi2=VHi*2 Lo2=VLo*2
VAC %AC %Step ACMag=ABS(V.Hi2-V.Lo2) ACPH=0 DC=0
X10PoleLP1 %In %Step
+ '10PoleLP' (.349/tr )
Rs %AC %Out VALUE=Zo
VStep %In %0 TRAN=Pulse(V.Lo2 V.Hi2 td )
.ENDS 'StepGen'

.SUBCKT '10PoleLP'
+ %In %Out
+ (Fc)
# 10 Pole Gaussian low pass filter, noisy R's
.PARAM G R=1 C=1/(R*TwoPi*Fc) L=R/(TwoPi*Fc)
R_Load %GOut %0 VALUE=G.R
R_Source %10 %A VALUE=G.R
R_In %In %0 1E15
EIn %10 %0 %In %0 2
EOut %Out %0 %GOut %0 1
L7 %D %E VALUE=0.6244*G.L
L9 %E %GOut VALUE=1.0147*G.L
L1 %A %B VALUE=0.0512*G.L
L3 %B %C VALUE=0.2509*G.L
L5 %C %D VALUE=0.4353*G.L
C10 %GOut %0 VALUE=2.2594*G.C
C6 %D %0 VALUE=0.5250*G.C
C8 %E %0 VALUE=0.7597*G.C
C2 %B %0 VALUE=0.1525*G.C
C4 %C %0 VALUE=0.3451*G.C
.ENDS '10PoleLP'

*****

.END

```

i. Frequency Analysis

```
*****
* Name:          Frequency Domain Analysis of PCB Via          *
*                                                       *
* Student:       Brock J. LaMeres                             *
*               University of Colorado                         *
*               Electrical and Computer Engineering Department *
*                                                       *
* Begin Date:    August 1999                                  *
* End Date:      July   2000                                  *
*                                                       *
* Purpose:       This SPICE deck models the S-parameter       *
*               analysis of the pcb via equivalent circuit.   *
*               The empirical data measured using a Network Analyzer *
*               is also displayed.                             *
*                                                       *
*****
```

```
.OPTION Map
.AC LIN 801 6Meg 6G
```

```
***** Parameters *****
```

```
.PARAM Clumped = 199f
.PARAM Llumped = 363p
```

```
.PARAM Ccon = 1p
.PARAM Lcon = 1p
```

```
*** This is the test circuit to look at simulation results *****
```

```
Vac %Vac_sweep %0 ACMag=1 ACPh=0 DC=0
Rs  %Vac_sweep %Vsim_s11 VALUE=50
```

```
Lcon1 %vsim_s11 %500 VALUE=Lcon
Ccon1 %vsim_s11 %0 VALUE=Ccon
```

```
Tlump1 %500 %0 %999 %0 Z0=75 td=200p
```

```
*Clump1 %999 %0 VALUE=Clumped/2
*Llump1 %999 %997 VALUE=Llumped
*Clump2 %997 %0 VALUE=Clumped/2
```

```
Tlump3 %999 %0 %400 %0 Z0=75 td=200p
```

```
Ccon2 %vsim_s21 %0 VALUE=Ccon
Lcon2 %400 %vsim_s21 VALUE=Lcon
```

```
Tinf %vsim_s21 %0 %vinfi %0 Z0=50 td=3.5n
Rinfi %vinfi %0 50
```

```
*** This is the circuit for looking at Network Analyzer Results
```

```
Vna1_s11 %V_file1_s11 %0 TRAN=PWL(
.INCLUDE "../NA_Results/Via1_NA.s11")
Rfile1_s11 %V_file1_s11 %0 VALUE=50
```

```
Vna1_s21 %V_file1_s21 %0 TRAN=PWL(
.INCLUDE "../NA_Results/Via1_NA.s21")
Rfile1_s21 %V_file1_s21 %0 VALUE=50
```

```
.END
```